(12) UK Patent Application (19) GB (11) 2 280 575 (13) A

(43) Date of A Publication 01.02.1995

(21) Application No 9317205.4

(22) Date of Filing 18.08.1993

(30) Priority Data
(31) 9315845 (32) 30.07.1993 (33) GB

(71) Applicant(s)
Roke Manor Research Limited

(Incorporated in the United Kingdom)

Roke Manor, Old Salisbury Lane, ROMSEY, Hampshire, SO51 0ZN, United Kingdom

(72) Inventor(s)
Anthony Peter Hulbert

(74) Agent and/or Address for Service
Derek Allen
Siemens Group Services Limited, Intellectual Property Department, Roke Manor, Old Salisbury Lane, ROMSEY, Hampshire, SO51 0ZN, United Kingdom

(51) INT CL[6]
H04L 27/227 , H04J 13/00 13/02

(52) UK CL (Edition N)
H4P PAL PDCSL
U1S S2204 S2213

(56) Documents Cited
None

(58) Field of Search
UK CL (Edition L) H4L LBSF , H4P PAL PAN PAQ PDCSL PRE PRR
INT CL[5] H04B 7/216 , H04J 13/00 , H04L 27/22 27/30 27/38
ONLINE DATABASES : WPI

(54) A digital radio link using direct sequence spread spectrum.

(57) The apparatus comprises a comprehensive Rake cancellor, in which a complex baseband input signal is received by a pilot based estimator 43 which is arranged to generate output signals for application to a complex Rake filter and also a signal indicative of measured pilot energy. The complex Rake filter has its output 42 de-randomised and is fed to at least two interferer de-modulator and re-modulators 56, 58, which are controlled by a scaled version 60 of the measured pilot energy signal 52. The output signals from the interferer de-modulator and re-modulators are phase randomised 64 and subjected to interference processing by a channel model circuit 70. The output of the channel model circuit is subtracted from the baseband input signal and applied to a further complex Rake filter the output of which is further de-randomised. The reconstructed received data signals are generated from the output of the phase de-randomised 72 by real signal correlators 76, 78.

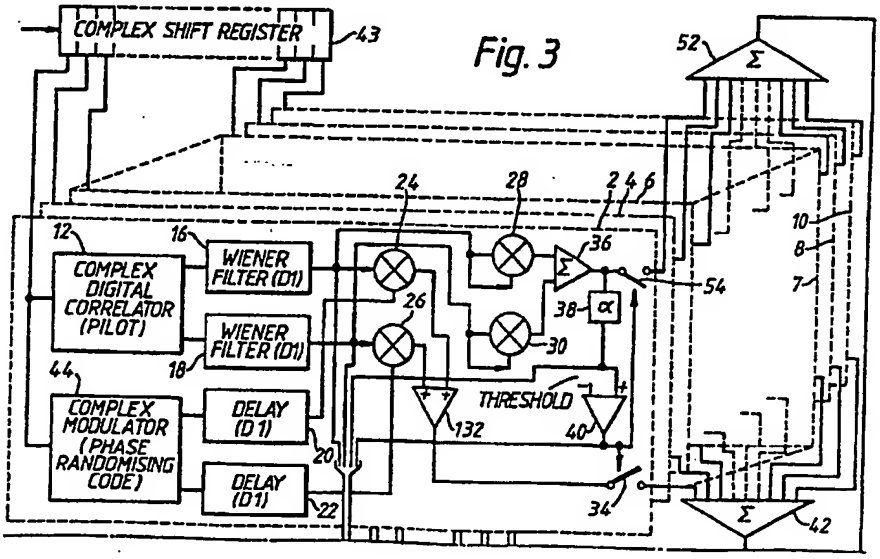
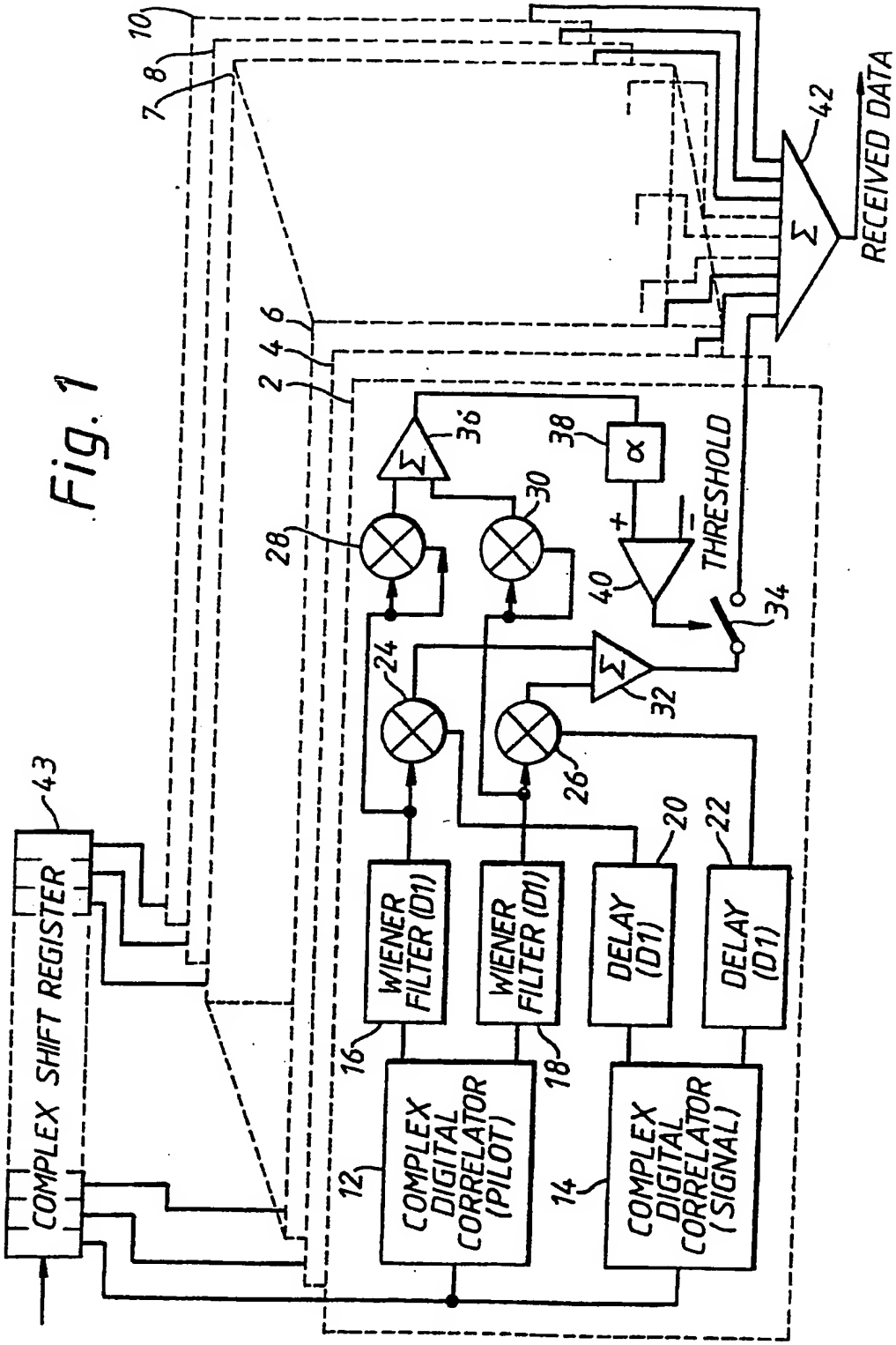


Fig. 3

GB 2 280 575 A

Fig. 1


10
7 8
42
RECEIVED DATA
Σ
2 4 6
36
38
α
THRESHOLD
30
28
40
34
24
32
26
20
22
43
WIENER FILTER (D1)
WIENER FILTER (D1)
DELAY (D1)
DELAY (D1)
16
18
COMPLEX SHIFT REGISTER
12
COMPLEX DIGITAL CORRELATOR (PILOT)
14
COMPLEX DIGITAL CORRELATOR (SIGNAL)

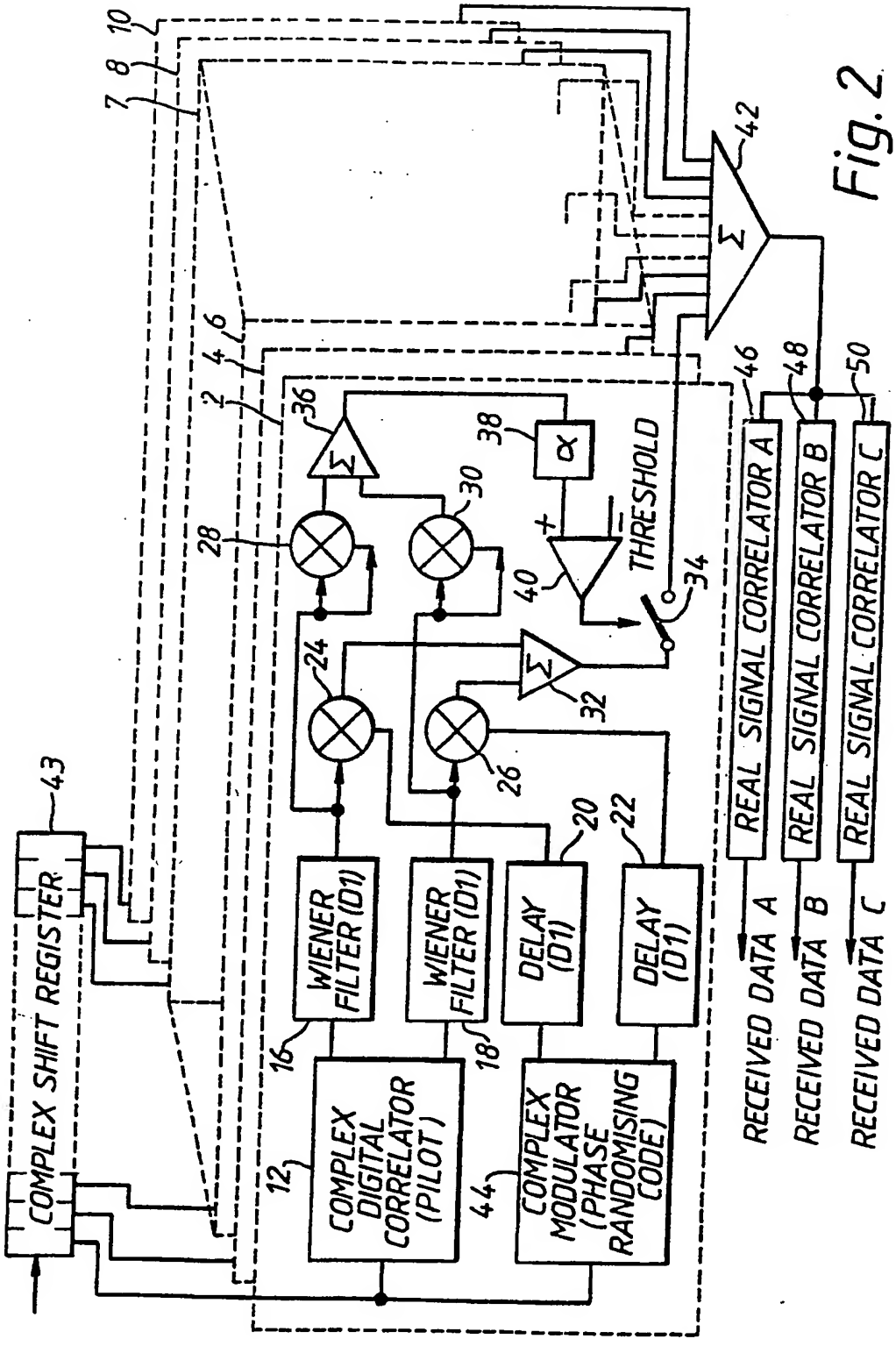

COMPLEX SHIFT REGISTER
43
COMPLEX DIGITAL CORRELATOR (PILOT)
12
COMPLEX MODULATOR (PHASE RANDOMISING CODE)
44
WIENER FILTER (D1)
16
WIENER FILTER (D1)
18
DELAY (D1)
20
DELAY (D1)
22
24
26
28
30
32
36
38
40
THRESHOLD
34
42
REAL SIGNAL CORRELATOR A
46
REAL SIGNAL CORRELATOR B
48
REAL SIGNAL CORRELATOR C
50
RECEIVED DATA A
RECEIVED DATA B
RECEIVED DATA C
2
4
6
7
8
10

Fig. 2

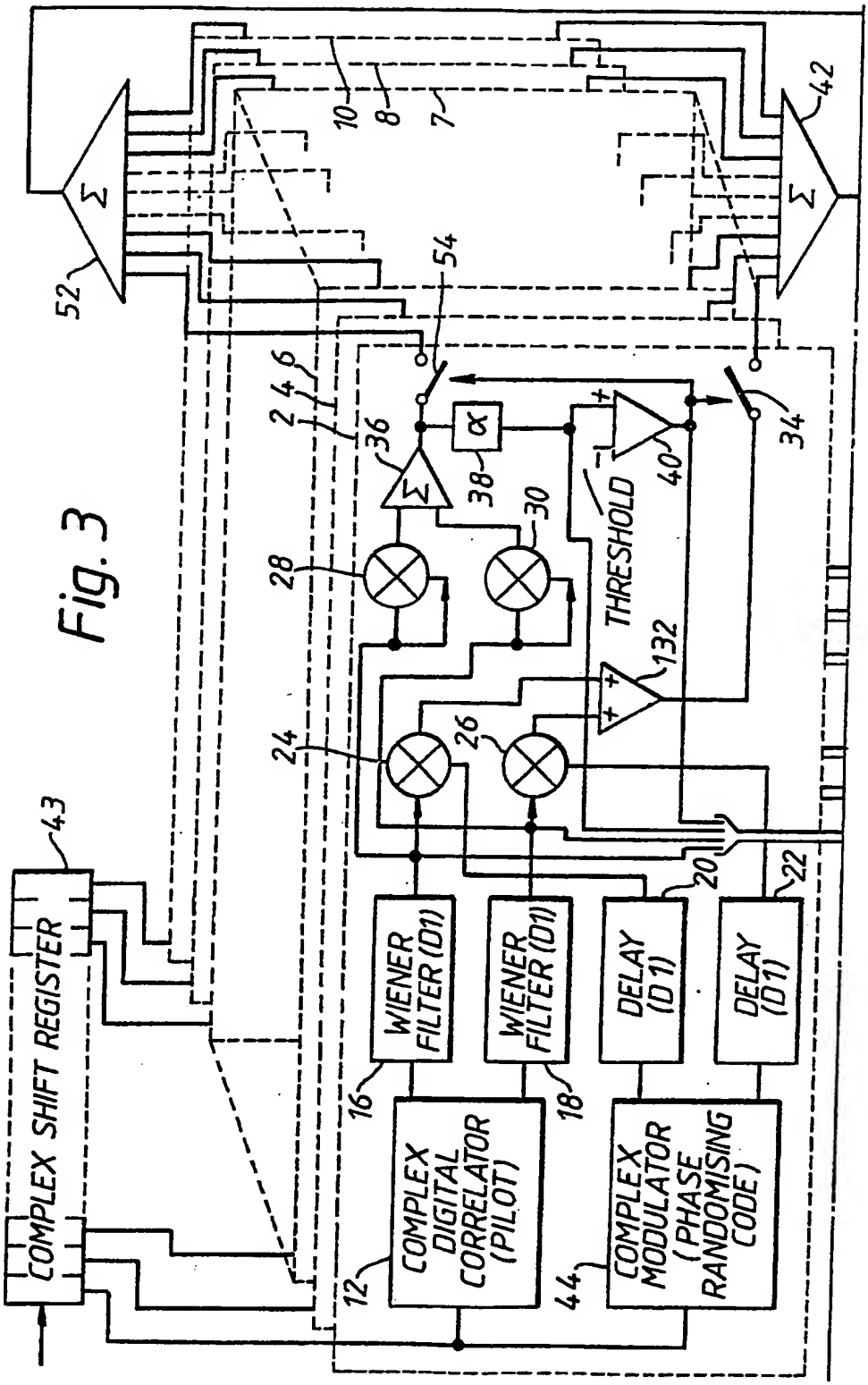

COMPLEX SHIFT REGISTER
43
COMPLEX DIGITAL CORRELATOR (PILOT)
12
WIENER FILTER (D1)
16
WIENER FILTER (D1)
18
DELAY (D1)
20
DELAY (D1)
22
COMPLEX MODULATOR (PHASE RANDOMISING CODE)
44
THRESHOLD
132
Σ
α
52
54
42
34
36
38
40
30
28
24
26
10
8
7
2 4 6
1

Fig. 3

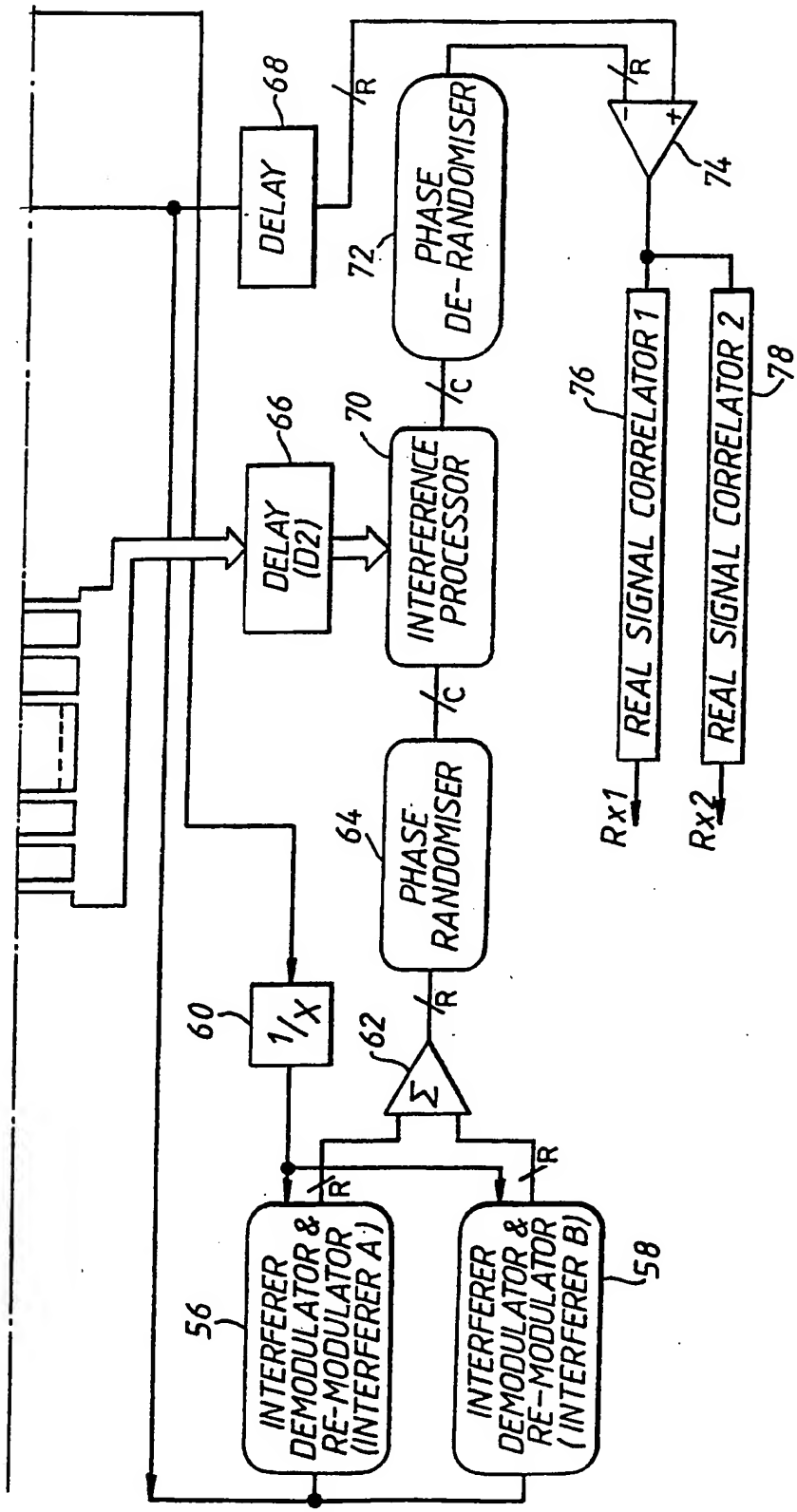

INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A)
56
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B)
58
1/X
60
Σ
62
PHASE RANDOMISER
64
DELAY (D2)
66
DELAY
68
INTERFERENCE PROCESSOR
70
PHASE DE-RANDOMISER
72
74
REAL SIGNAL CORRELATOR 1
76
REAL SIGNAL CORRELATOR 2
78
Rx1
Rx2
R
C

Fig. 3 cont.

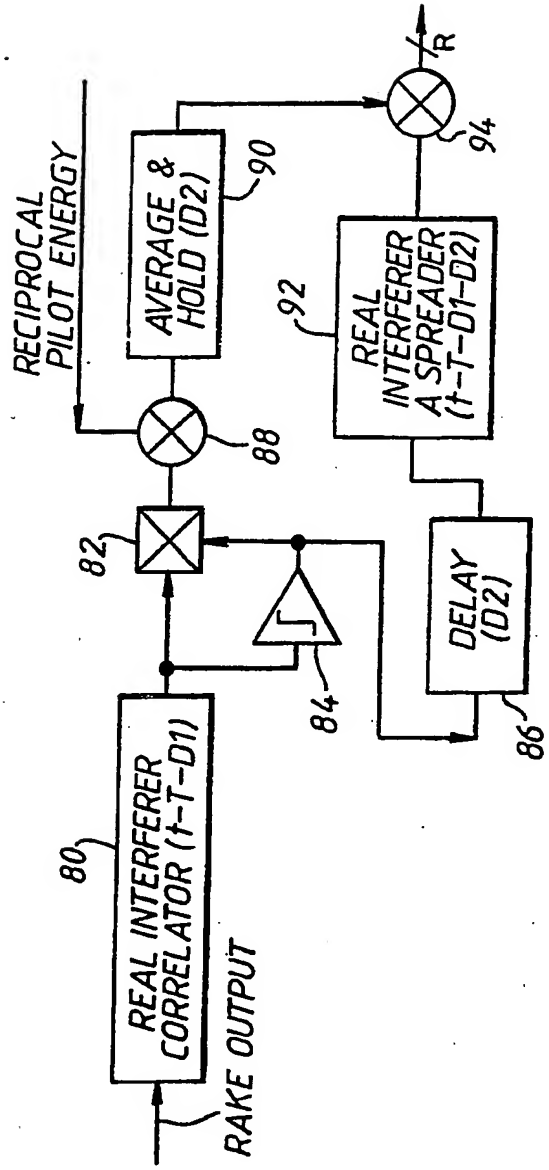

RECIPROCAL PILOT ENERGY
AVERAGE & HOLD (D2)
90
REAL INTERFERER A SPREADER (1-T-D1-D2)
92
R
94
88
82
84
DELAY (D2)
86
REAL INTERFERER CORRELATOR (1-T-D1)
80
RAKE OUTPUT

Fig. 4

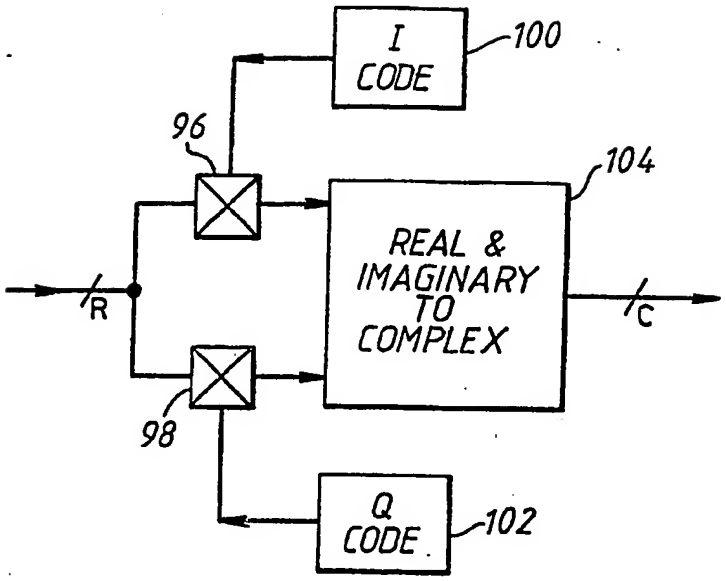

I
CODE
100
96
104
REAL &
IMAGINARY
TO
COMPLEX
R
C
98
Q
CODE
102

Fig. 5

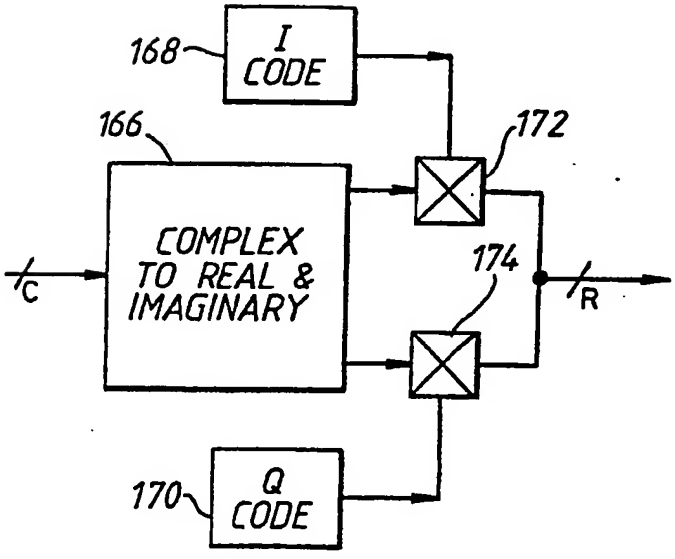

168
I
CODE
166
172
COMPLEX
TO REAL &
IMAGINARY
174
C
R
170
Q
CODE

Fig. 8

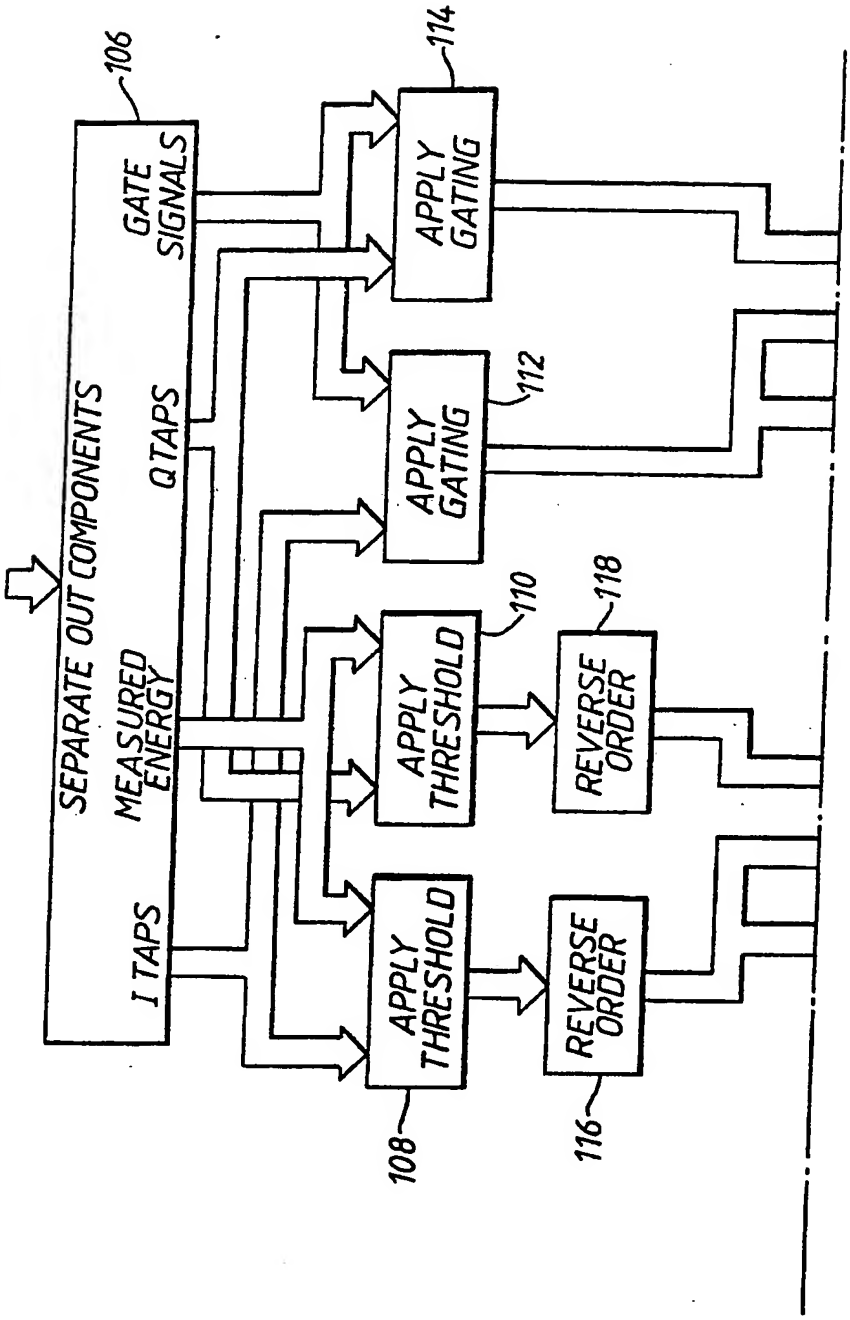

106
SEPARATE OUT COMPONENTS
MEASURED ENERGY
I TAPS
Q TAPS
GATE SIGNALS
114
APPLY GATING
112
APPLY GATING
110
APPLY THRESHOLD
118
REVERSE ORDER
108
APPLY THRESHOLD
116
REVERSE ORDER

Fig. 6

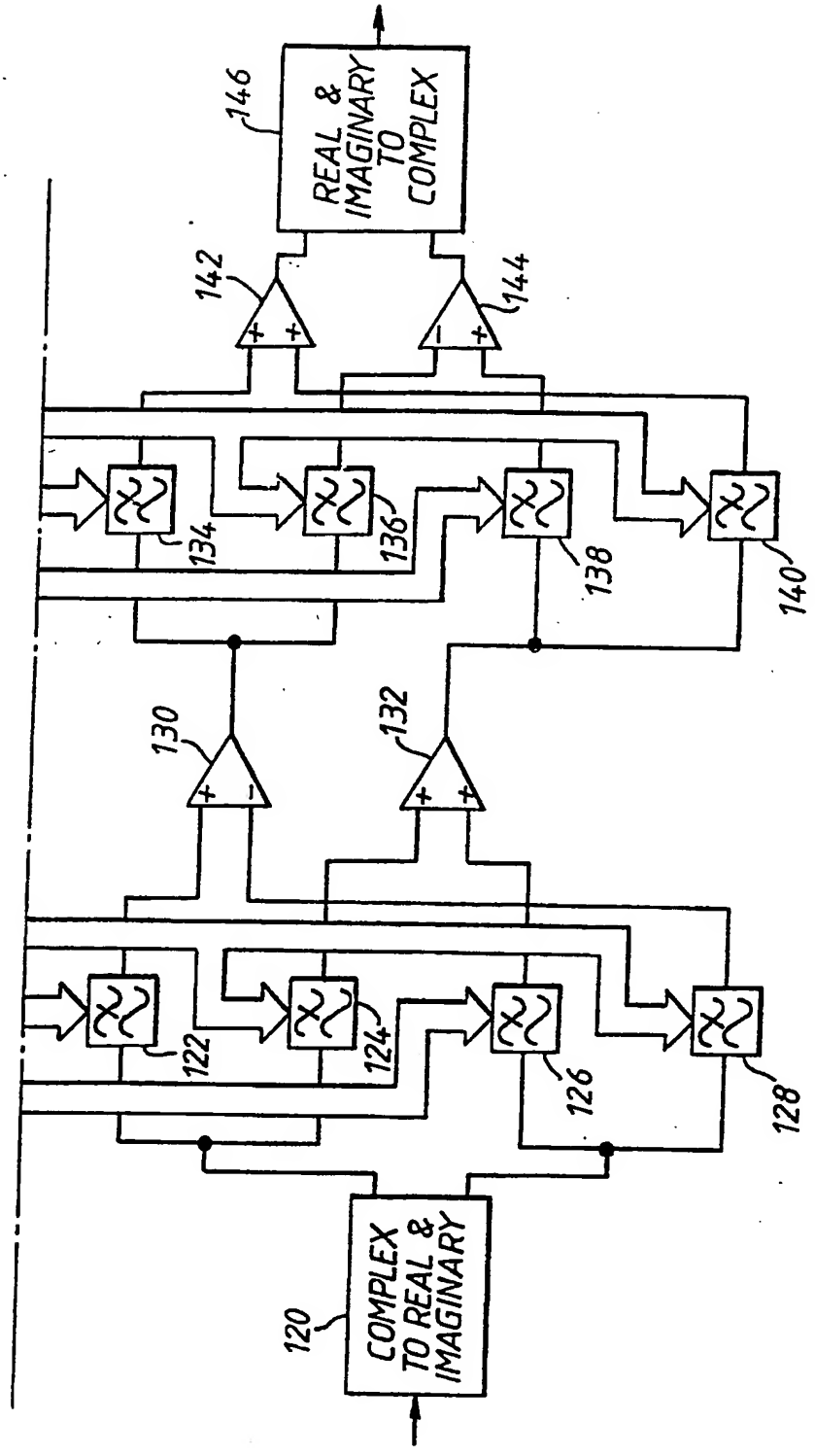

REAL & IMAGINARY TO COMPLEX
146
142
144
134
136
138
140
130
132
122
124
126
128
COMPLEX TO REAL & IMAGINARY
120

Fig. 6 cont.

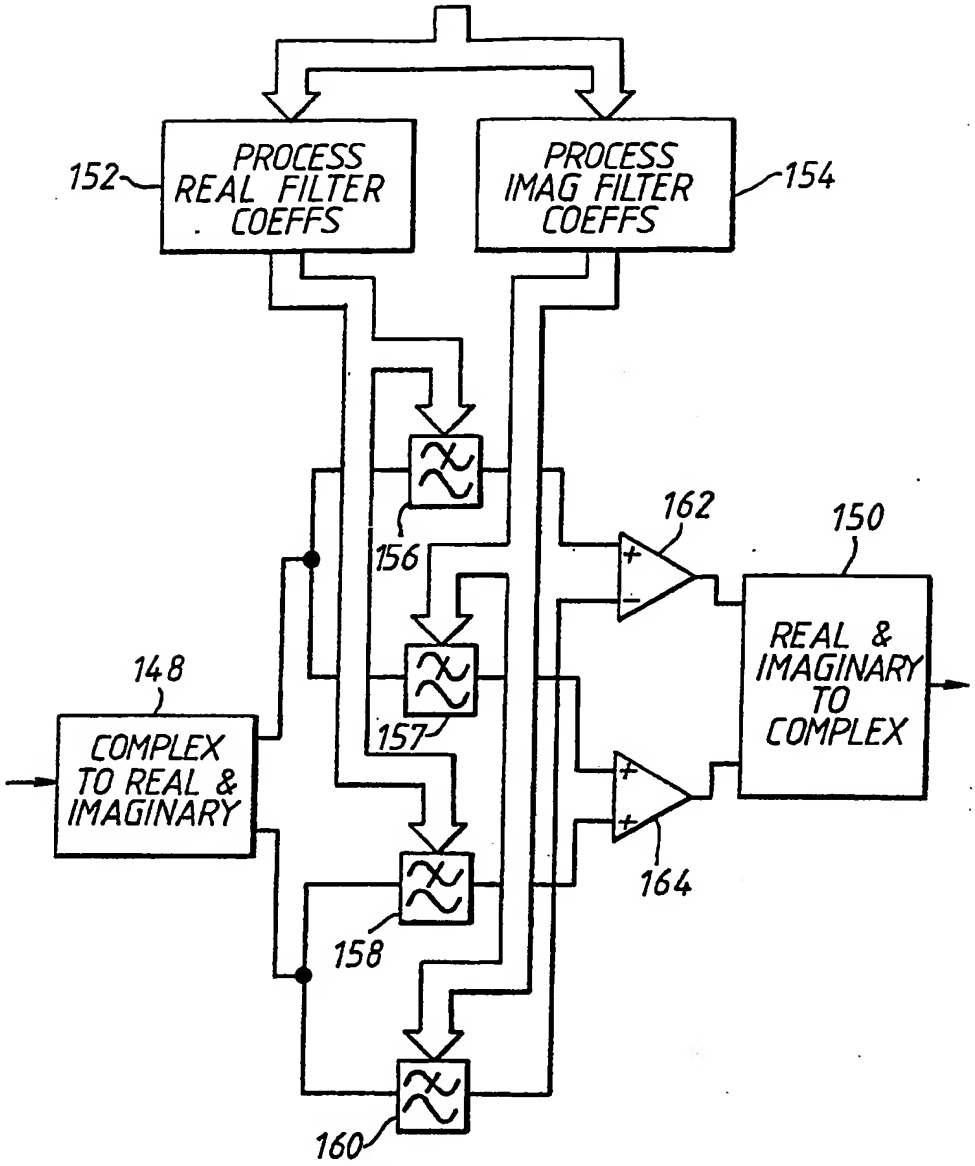

PROCESS REAL FILTER COEFFS
PROCESS IMAG FILTER COEFFS
152
154
156
157
158
160
162
164
150
148
COMPLEX TO REAL & IMAGINARY
REAL & IMAGINARY TO COMPLEX

Fig. 7

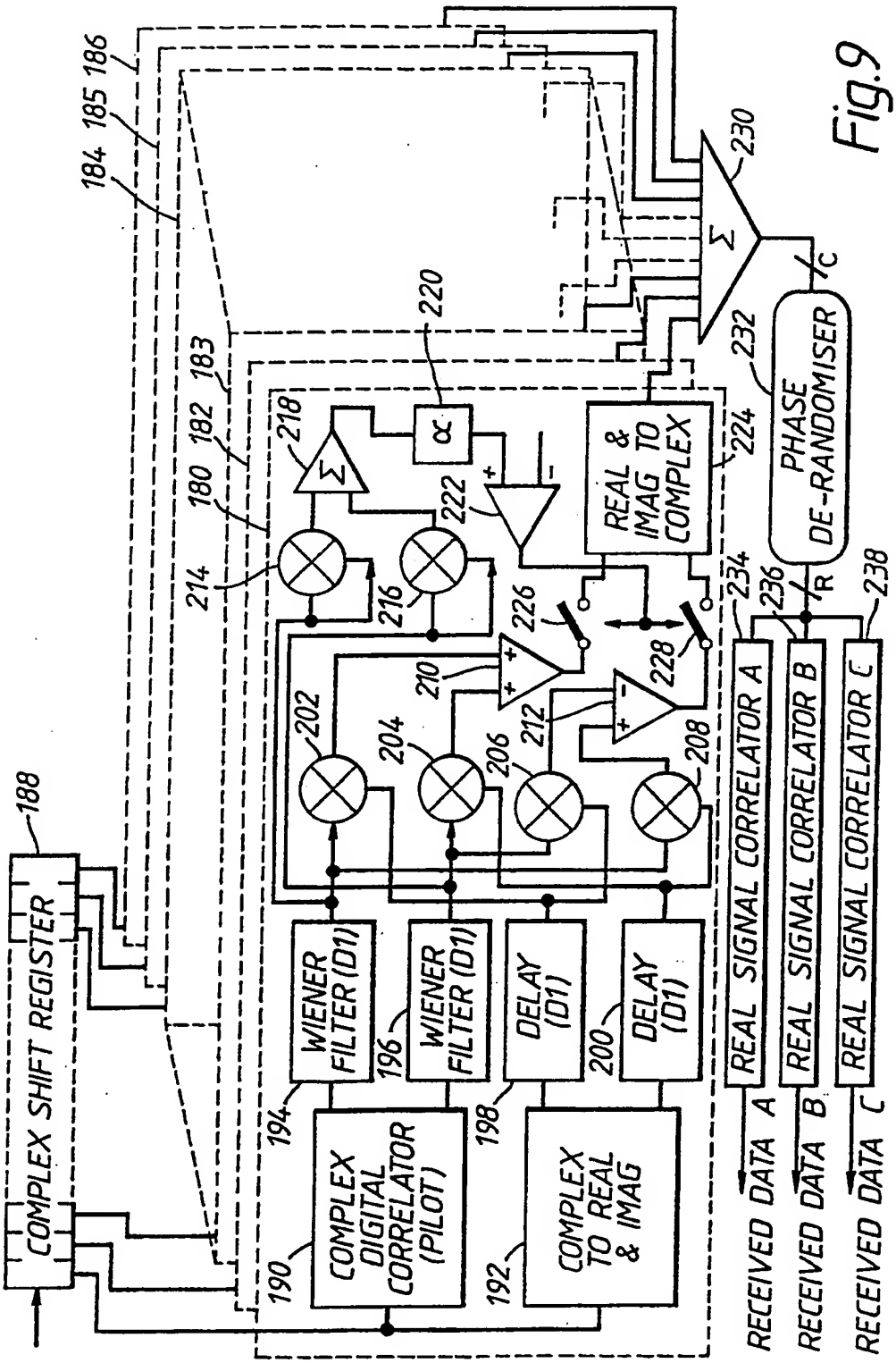
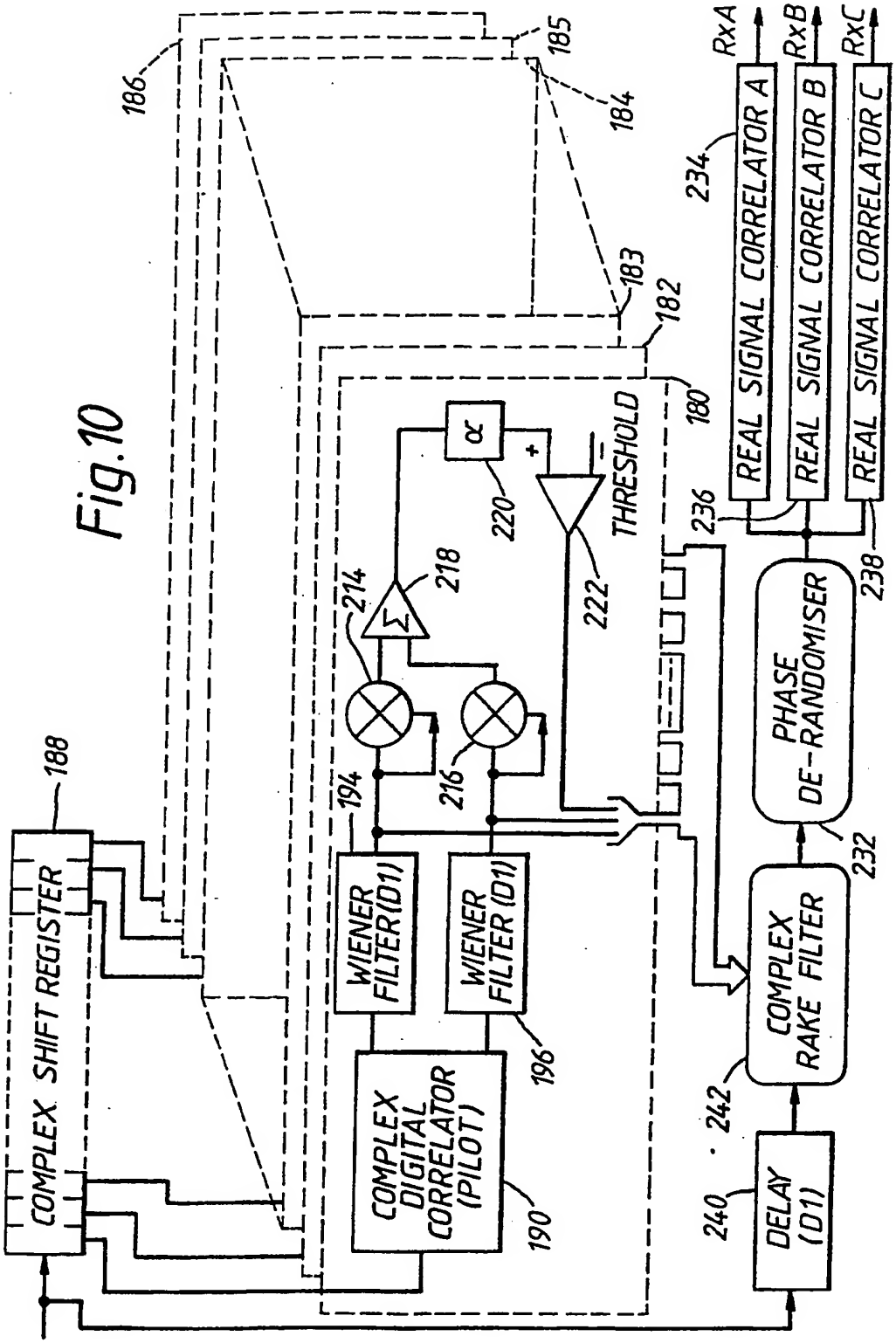

COMPLEX SHIFT REGISTER
188
184
185
186
183
182
180
214
216
218
220
222
224
226
228
230
232
234
236
238
202
204
206
208
210
212
WIENER FILTER (D1)
196
WIENER FILTER (D1)
DELAY (D1)
200
DELAY (D1)
194
198
COMPLEX DIGITAL CORRELATOR (PILOT)
190
COMPLEX TO REAL & IMAG
192
REAL & IMAG TO COMPLEX
PHASE DE-RANDOMISER
REAL SIGNAL CORRELATOR A
REAL SIGNAL CORRELATOR B
REAL SIGNAL CORRELATOR C
RECEIVED DATA A
RECEIVED DATA B
RECEIVED DATA C

Fig.9

Fig.10


186
185
184
183
182
180
188
COMPLEX SHIFT REGISTER
194
WIENER FILTER(D1)
WIENER FILTER (D1)
196
COMPLEX DIGITAL CORRELATOR (PILOT)
190
214
218
216
220
α
+
−
THRESHOLD
222
236
234
REAL SIGNAL CORRELATOR A
REAL SIGNAL CORRELATOR B
REAL SIGNAL CORRELATOR C
RxA
RxB
RxC
238
PHASE DE-RANDOMISER
232
COMPLEX RAKE FILTER
242
240
DELAY (D1)

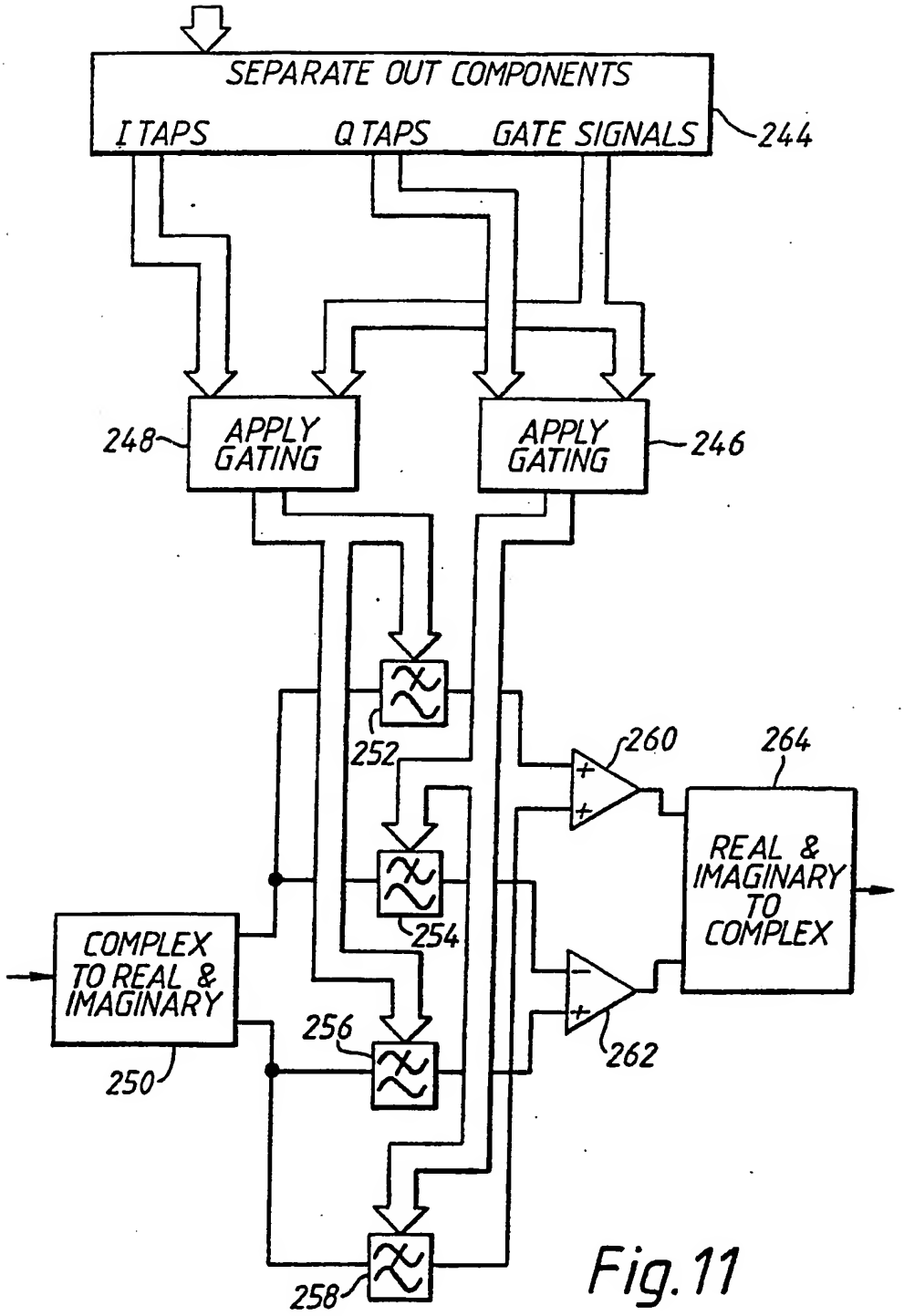

SEPARATE OUT COMPONENTS
I TAPS
Q TAPS
GATE SIGNALS
244
248
APPLY GATING
APPLY GATING
246
252
254
256
258
260
262
264
REAL & IMAGINARY TO COMPLEX
COMPLEX TO REAL & IMAGINARY
250

Fig. 11

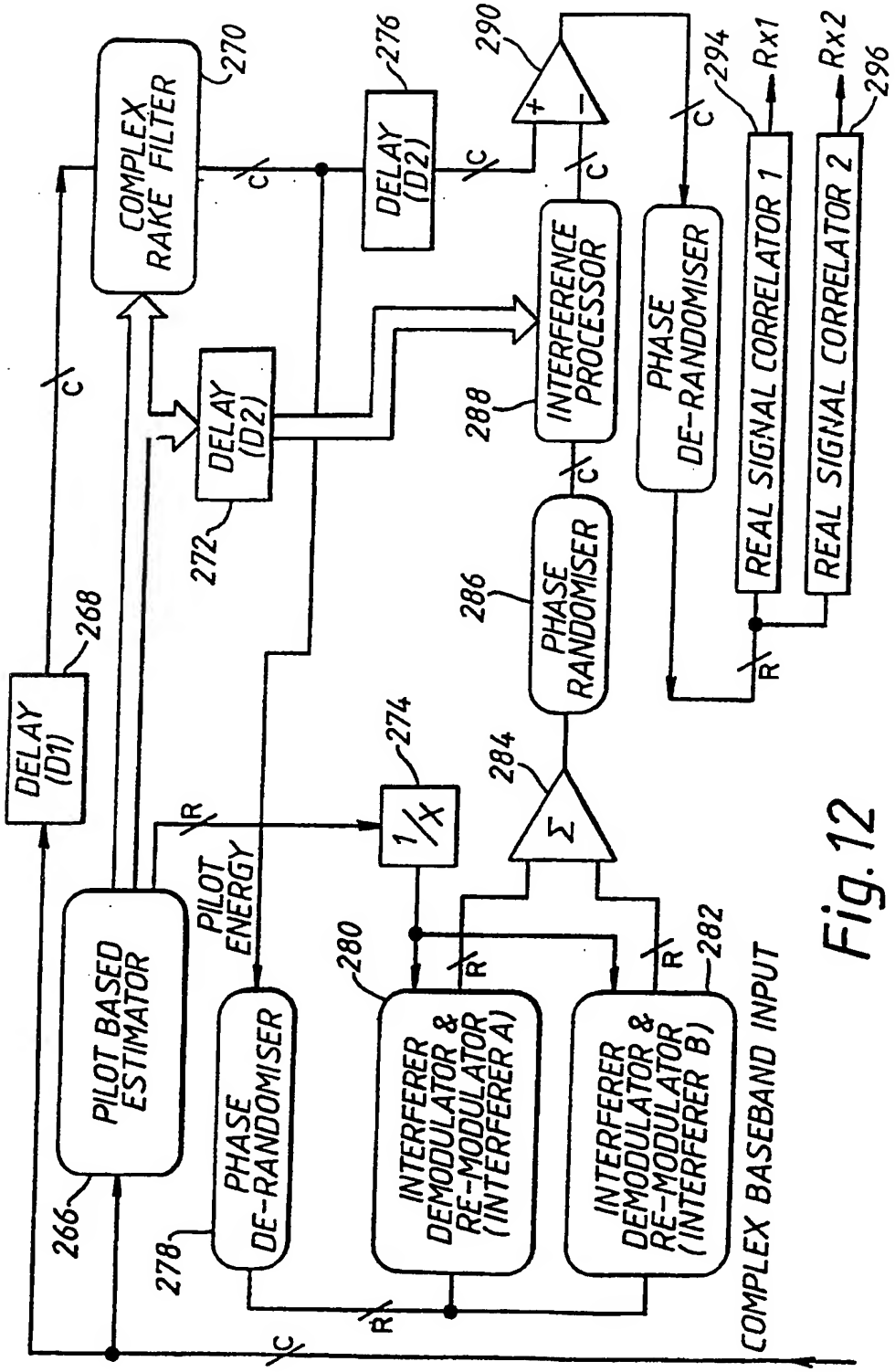

COMPLEX BASEBAND INPUT
PILOT BASED ESTIMATOR
266
DELAY (D1)
268
COMPLEX RAKE FILTER
270
DELAY (D2)
272
PILOT ENERGY
PHASE DE-RANDOMISER
278
1/X
274
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A)
280
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B)
282
Σ
284
PHASE RANDOMISER
286
INTERFERENCE PROCESSOR
288
DELAY (D2)
276
+
−
290
PHASE DE-RANDOMISER
294
REAL SIGNAL CORRELATOR 1
Rx1
REAL SIGNAL CORRELATOR 2
Rx2
296
C
R

Fig. 12

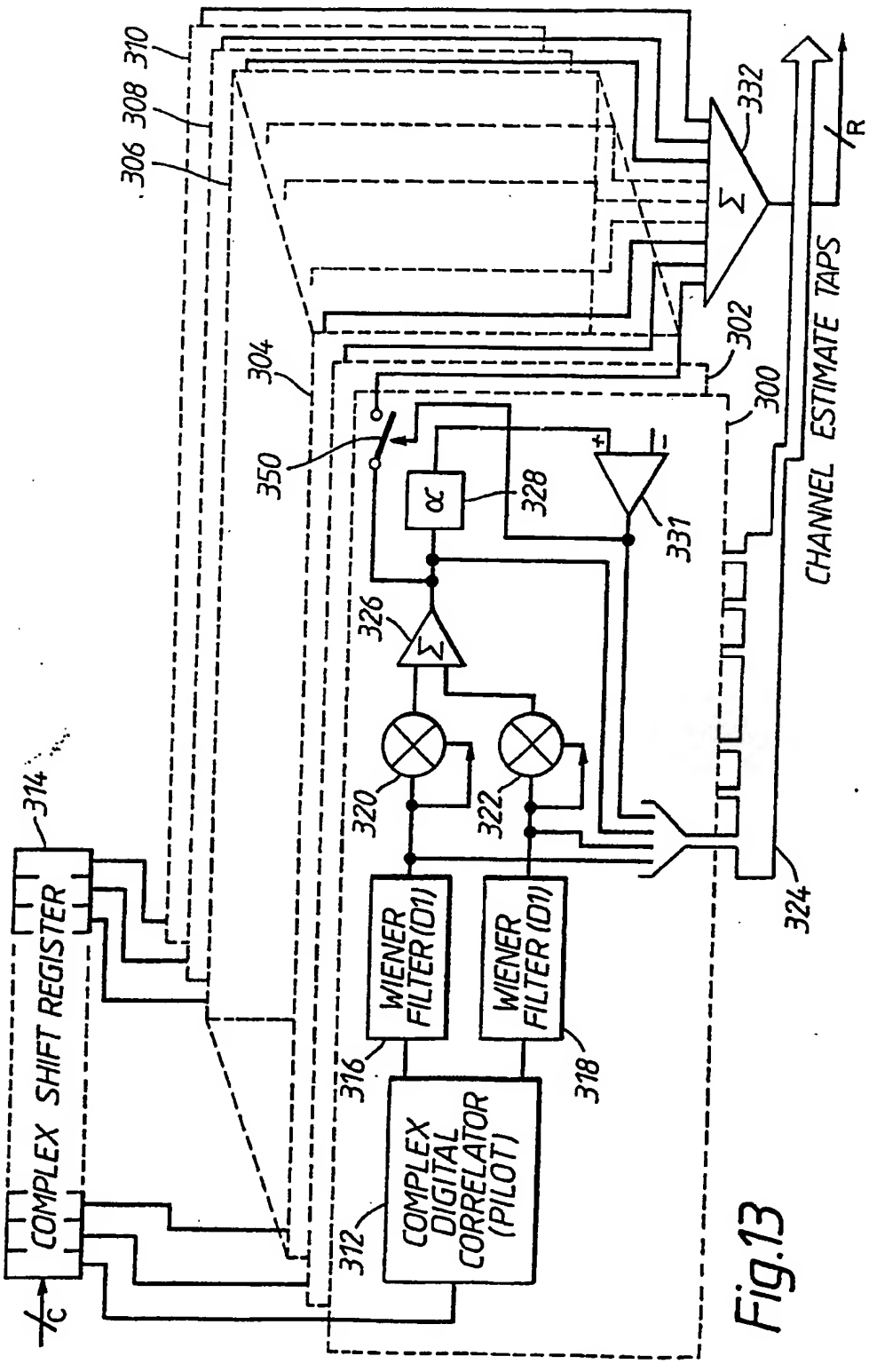

310
308
306
304
302
300
332
R
CHANNEL ESTIMATE TAPS
Σ
350
α
328
331
326
320
322
314
COMPLEX SHIFT REGISTER
WIENER FILTER (D1)
WIENER FILTER (D1)
316
318
COMPLEX DIGITAL CORRELATOR (PILOT)
312
C
324

Fig.13

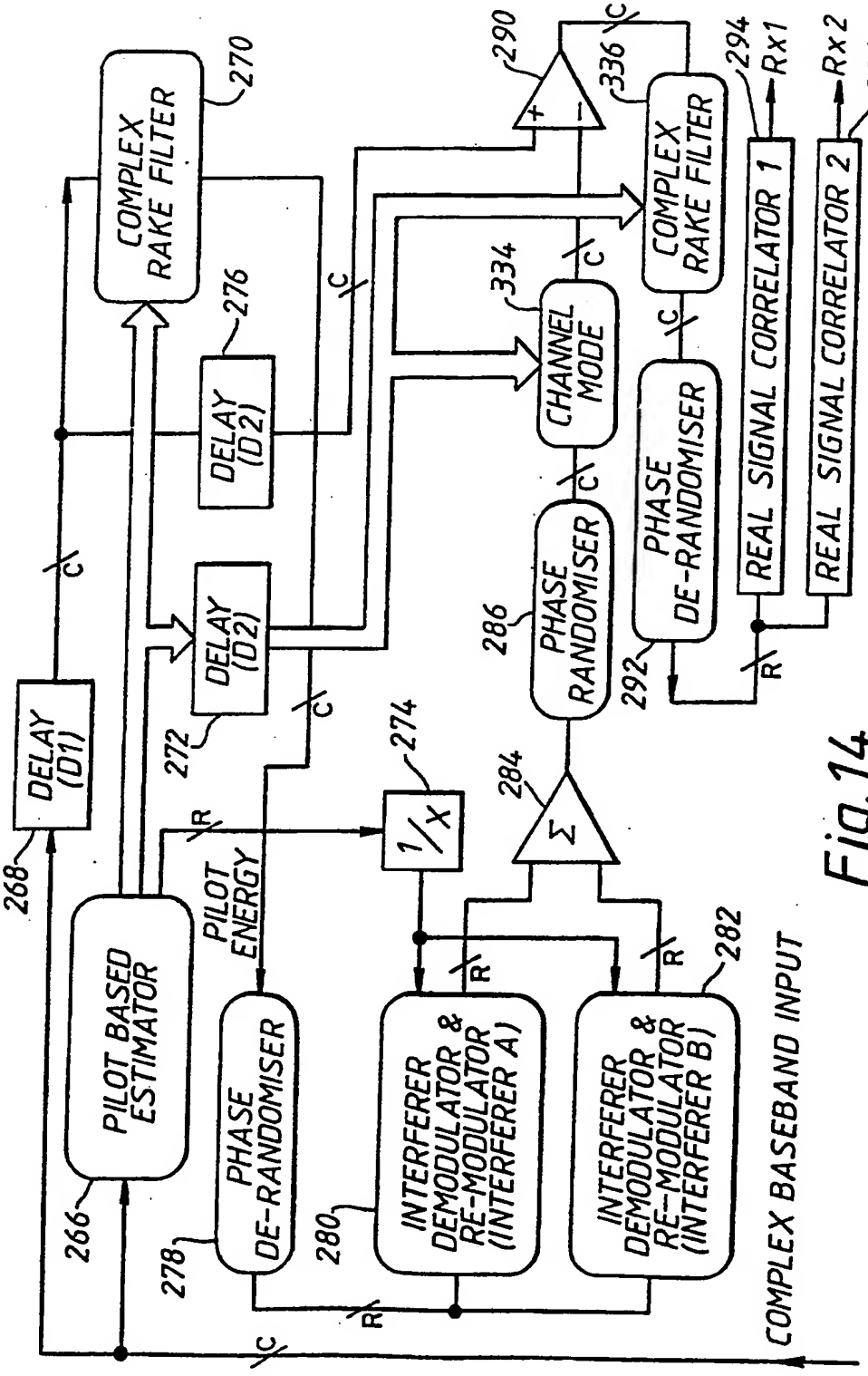

COMPLEX BASEBAND INPUT
PILOT BASED ESTIMATOR
266
DELAY (D1)
268
COMPLEX RAKE FILTER
270
DELAY (D2)
272
DELAY (D2)
276
PILOT ENERGY
1/X
274
PHASE DE-RANDOMISER
278
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A)
280
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B)
282
Σ
284
PHASE RANDOMISER
286
CHANNEL MODE
334
+
−
290
336
COMPLEX RAKE FILTER
PHASE DE-RANDOMISER
292
REAL SIGNAL CORRELATOR 1
294
Rx1
REAL SIGNAL CORRELATOR 2
Rx2
296
C
R

Fig. 14

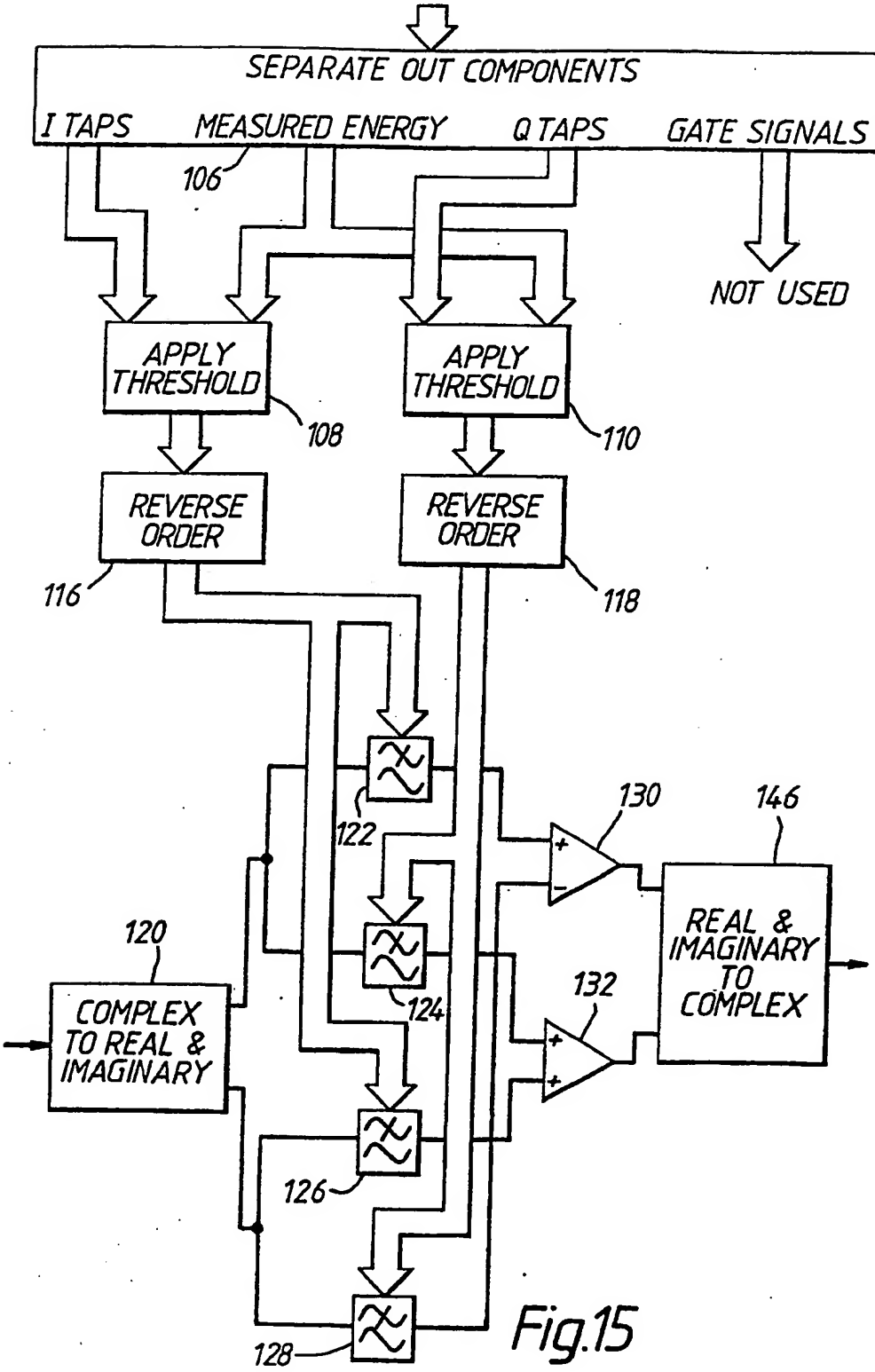

SEPARATE OUT COMPONENTS
I TAPS
MEASURED ENERGY
Q TAPS
GATE SIGNALS
106
NOT USED
APPLY THRESHOLD
108
APPLY THRESHOLD
110
REVERSE ORDER
116
REVERSE ORDER
118
122
130
146
120
COMPLEX TO REAL & IMAGINARY
124
132
REAL & IMAGINARY TO COMPLEX
126
128

Fig.15

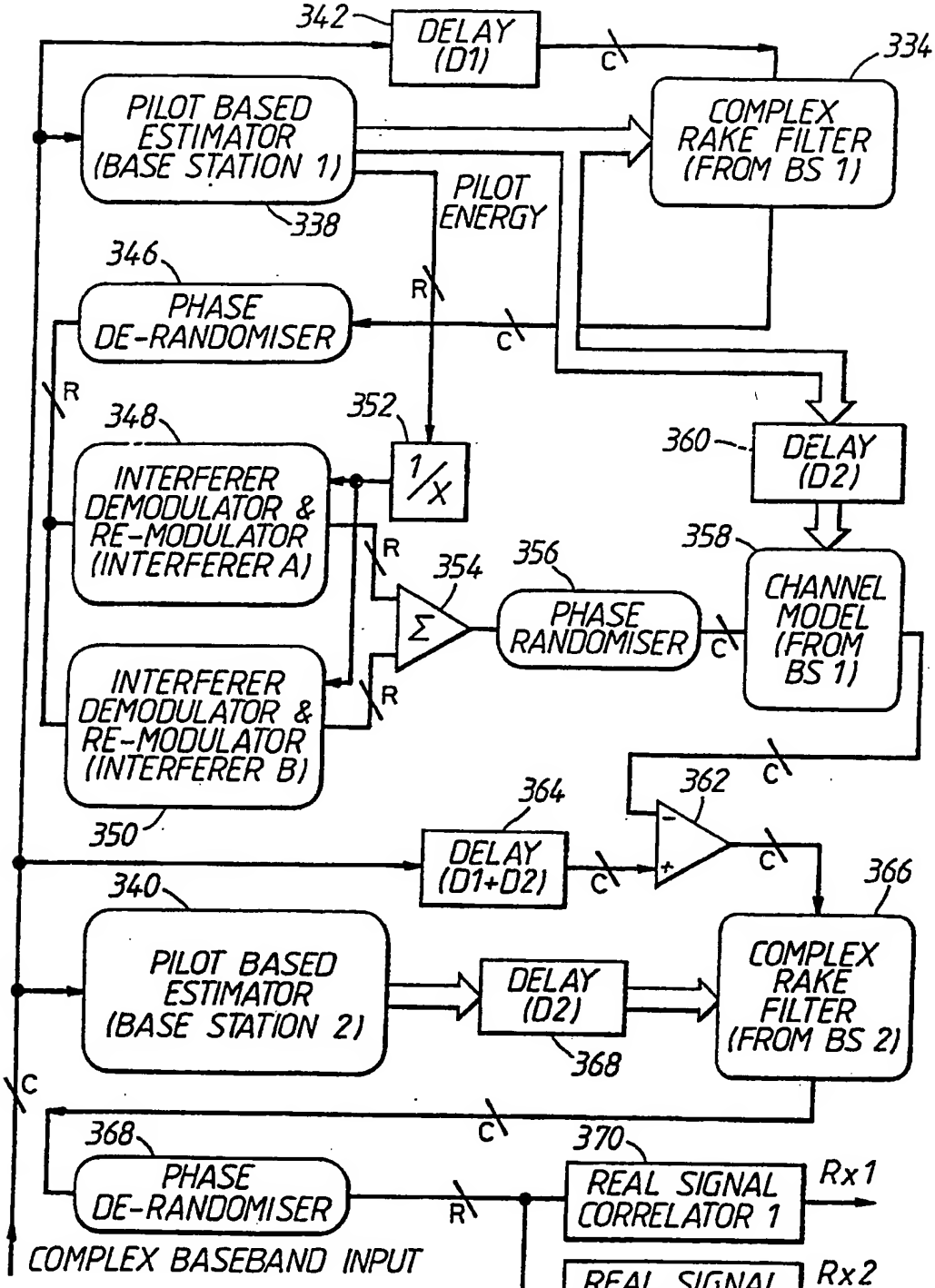

342
DELAY (D1)
C
334
PILOT BASED ESTIMATOR (BASE STATION 1)
338
COMPLEX RAKE FILTER (FROM BS 1)
PILOT ENERGY
346
PHASE DE-RANDOMISER
R
C
R
348
352
1/x
360
DELAY (D2)
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A)
R
354
Σ
356
PHASE RANDOMISER
C
358
CHANNEL MODEL (FROM BS 1)
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B)
R
350
C
362
364
DELAY (D1+D2)
C
C
366
340
PILOT BASED ESTIMATOR (BASE STATION 2)
DELAY (D2)
368
COMPLEX RAKE FILTER (FROM BS 2)
C
C
368
370
PHASE DE-RANDOMISER
R
REAL SIGNAL CORRELATOR 1
Rx1
REAL SIGNAL CORRELATOR 2
Rx2
372
COMPLEX BASEBAND INPUT

Fig.16

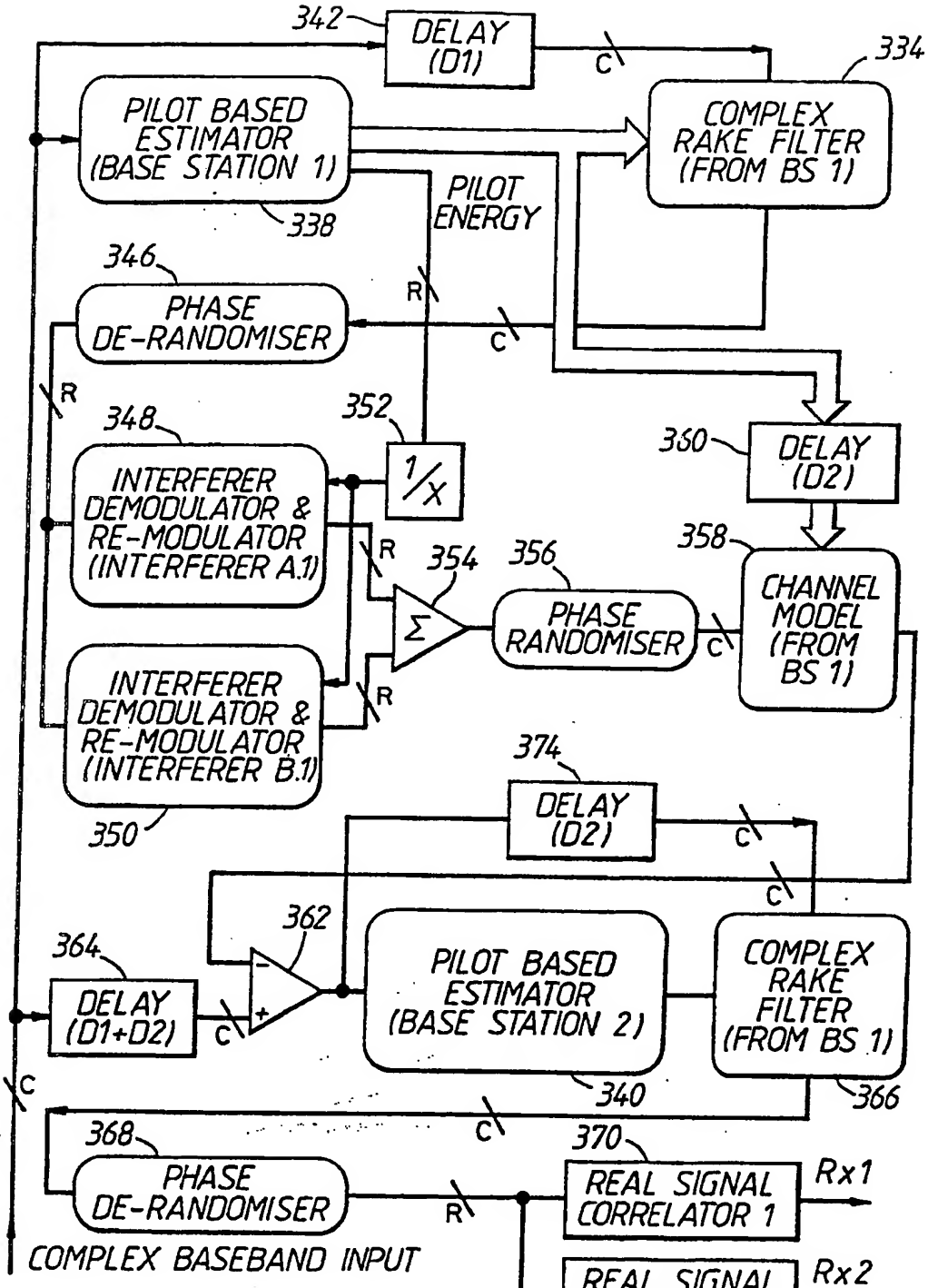

342
DELAY (D1)
C
334
PILOT BASED ESTIMATOR (BASE STATION 1)
COMPLEX RAKE FILTER (FROM BS 1)
338
PILOT ENERGY
346
PHASE DE-RANDOMISER
R
C
R
348
352
360
DELAY (D2)
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A.1)
1/X
358
R
354
356
Σ
PHASE RANDOMISER
CHANNEL MODEL (FROM BS 1)
C
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B.1)
R
374
DELAY (D2)
350
C
C
362
364
PILOT BASED ESTIMATOR (BASE STATION 2)
COMPLEX RAKE FILTER (FROM BS 1)
DELAY (D1+D2)
C
340
366
C
C
368
370
PHASE DE-RANDOMISER
R
REAL SIGNAL CORRELATOR 1
Rx1
COMPLEX BASEBAND INPUT
REAL SIGNAL CORRELATOR 2
Rx2
372

Fig.17

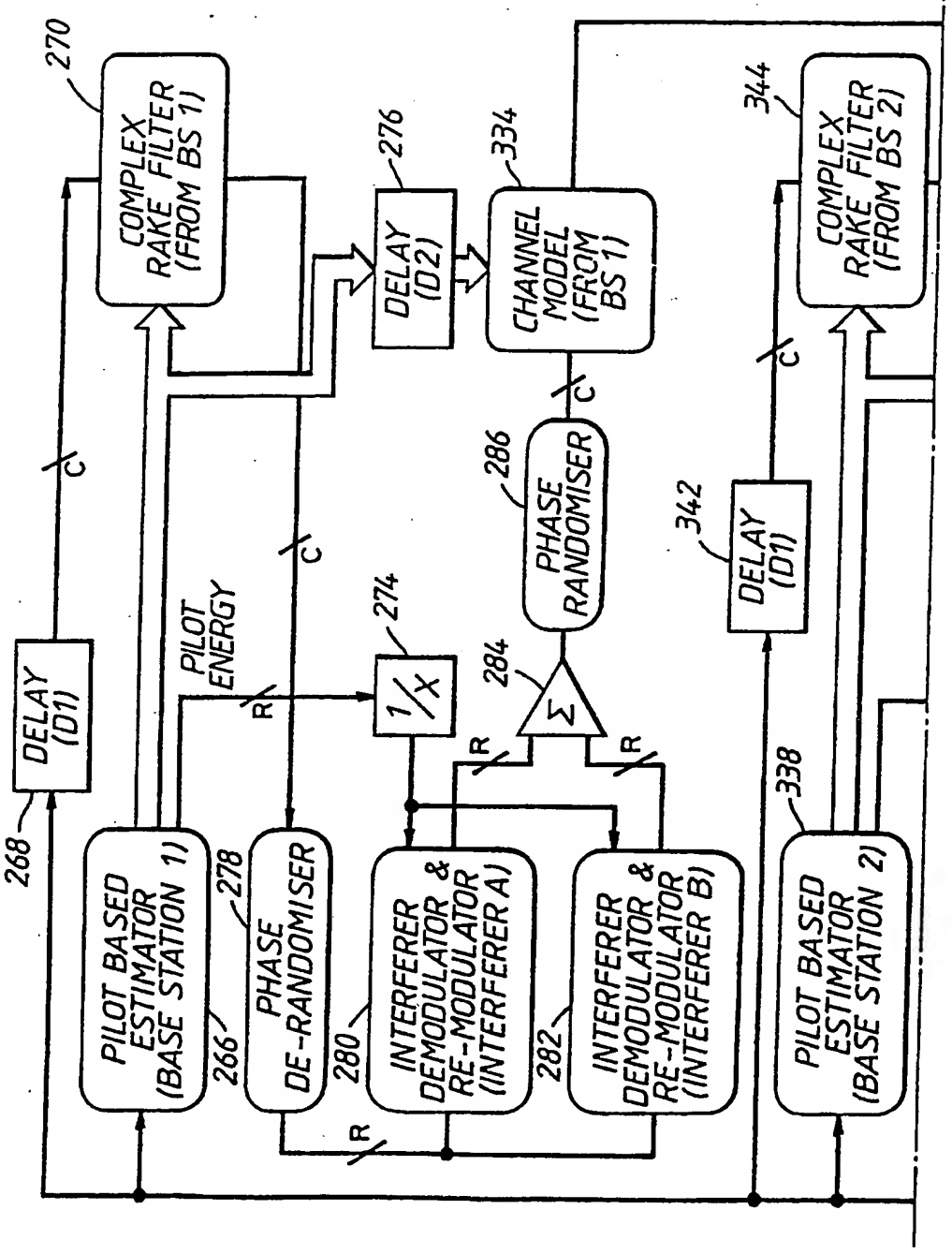

270
COMPLEX RAKE FILTER (FROM BS 1)
276
DELAY (D2)
334
CHANNEL MODEL (FROM BS 1)
344
COMPLEX RAKE FILTER (FROM BS 2)
C
C
C
C
DELAY (D1)
268
PILOT ENERGY
R
274
1/X
284
Σ
R
R
286
PHASE RANDOMISER
342
DELAY (D1)
PILOT BASED ESTIMATOR (BASE STATION 1)
266
278
PHASE DE-RANDOMISER
280
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A)
282
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B)
338
PILOT BASED ESTIMATOR (BASE STATION 2)
R

Fig.18

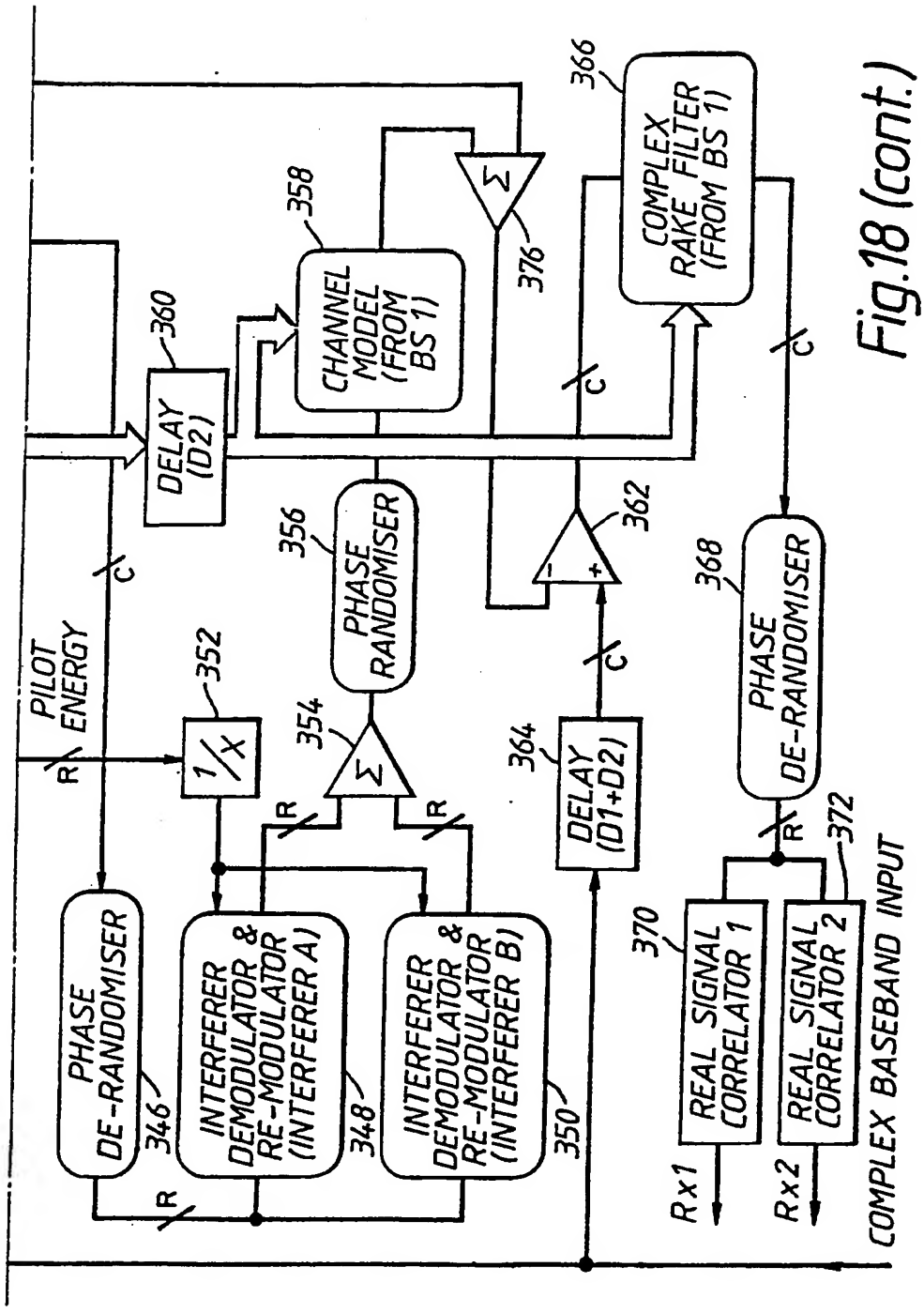

PILOT ENERGY
R
C
1/X
352
PHASE DE-RANDOMISER
346
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER A)
348
INTERFERER DEMODULATOR & RE-MODULATOR (INTERFERER B)
350
354
Σ
PHASE RANDOMISER
356
DELAY (D2)
360
CHANNEL MODEL (FROM BS 1)
358
Σ
376
COMPLEX RAKE FILTER (FROM BS 1)
366
362
DELAY (D1+D2)
364
PHASE DE-RANDOMISER
368
370
REAL SIGNAL CORRELATOR 1
372
REAL SIGNAL CORRELATOR 2
Rx1
Rx2
COMPLEX BASEBAND INPUT

Fig.18 (cont.)

2280575

APPARATUS FOR USE IN EQUIPMENT PROVIDING A DIGITAL RADIO LINK BETWEEN A FIXED AND A MOBILE RADIO UNIT

The present invention relates to apparatus for use in equipment providing a digital radio link between a fixed and a mobile radio unit.

GB Patent Application No 9313078.9 describes an invention using interference cancellation on the down-link of a CDMA Cellular Mobile Radio system to avoid the need for soft handoff (i.e. simultaneous transmission to a mobile from two or more base stations. GB Patent Application No 9311373.6 describes a Comprehensive Rake receiver in which a spread spectrum is processed, optimally to combine all significant multipath components. In architecture described in GB Patent Application No 9311373.6, digital correlators are provided over the multipath delay spread of the signal at one chip intervals and their outputs maximal ratio combined. With close to rectangular transmit and receive filters, almost the entire signal energy can be recovered at the output of the combiner, even though no attempt is made accurately to align any of the correlators onto specific multipath components.

The present invention combines the merits of the two previous inventions in a way which leads to benefits in performance and reductions in complexity. In particular, the Comprehensive Rake receiver lends itself well to the pre-combining Rake architecture which allows efficient reception (and

therefore cancellation) of multiple signals with modest complexity. Moreover, because the tap weights in the Rake processor automatically take account of the effect of the transmit and receive filters, there is no need to incorporate a combined filter in the reconstruction circuit. Also, the additional circuits for cancellation are almost identical to those for reception so that replication only, is required.

An object of the present invention is to provide Comprehensive Rake cancellation means which provides better performance and reduced complexity over known cancellation means.

According to the present invention there is provided apparatus for use in equipment providing a digital radio link, using direct sequence spread spectrum and including a pilot signal reference, between fixed and mobile radio units, said apparatus comprising a Rake receiver including a plurality of Rake fingers, each including means for measuring the amplitude of the pilot signal reference and means for weighting the amplitude in accordance with the measured pilot amplitude which cover a contiguous span of spreading code phases of the same order as the maximum delay spread of the signal to be received, first adder means connected to an output of each Rake finger and arranged to generate a combined output signal, correlation means connected to receive said combined output signal and arranged to demodulate said signal to reconstruct signals to be received, second adder means for generating a signal pertaining to total pilot signal energy, scaling means for scaling said total pilot energy signal,

and, means for cancelling interference from at least one interfering source of known spreading code, wherein said cancellation means is arranged to receive output signals from said first adder means and from said scaling means.

Various embodiments of the present invention will now be described with reference to the accompanying drawings, wherein,

FIGURE 1 shows a block diagram of a parallel comprehensive Rake receiver using Binary Phase Shift Keying with Quadrature Phase Shift Keying randomisation,

FIGURE 2 shows a block diagram of a pre-combining comprehensive Rake receiver,

FIGURE 3 shows a block diagram of an interference cancellor according to the present invention, based on a pre de-randomising comprehensive Rake receiver,

FIGURE 4 shows a block diagram of an interferer de-modulator and re-modulator shown in Figure 3,

FIGURE 5 shows a block diagram of a phase randomiser shown in Figure 3,

FIGURE 6 shows a block diagram of a interference processor shown in Figure 3,

FIGURE 7 shows a block diagram of an alternative interference processor shown in Figure 3,

FIGURE 8 shows a block diagram of a phase de-randomiser shown in Figure 3,

FIGURE 9 shows a block diagram of a pre-combining comprehensive Rake receiver which utilises post de-randomising,

FIGURE 10 shows a block diagram of a pre-combining comprehensive Rake receiver utilising post de-randomising and having finite impulse response filters,

FIGURE 11 shows a block diagram of a complex Rake filter shown in Figure 10,

FIGURE 12 shows a block diagram of an interference cancellor based on a pre-combining Rake receiver utilising post de-randomising,

FIGURE 13 shows a block diagram of a pilot based estimator shown in Figure 12,

FIGURE 14 shows a block diagram of an interference cancellor based on a pre-combining comprehensive Rake receiver utilising post de-randomising and pre-cancelling,

FIGURE 15 shows a block diagram of a channel model circuit shown in Figure 14,

FIGURE 16 shows a block diagram of an interference cancellor for use where the interference is generated from an other base station,

FIGURE 17 shows a block diagram of an alternative cancellor to that shown in Figure 16 and,

FIGURE 18 shows a block diagram of a cancellor where the interference is generated from two base stations.

In the description which follows, the modulation assumed is Binary Phase Shift Keying (BPSK) with Quadrature Phase Shift Keying (QPSK) randomisation. The latter is used to ensure constant interference to receivers of other signals, irrespective of the phase shift over the path. It is assumed that a common

randomising QPSK modulation sequence is applied to all of the signals transmitted from any particular base station. It will be appreciated by those versed in the art that the removal of the QPSK randomisation would not alter the substance of the invention and would in fact result in a simpler architecture.

For example, if QPSK randomisation is not employed, the complex filters become half complex filters.

In all of the block diagrams referred to, where relevant, a real (single line) connection between blocks is labelled with a R. A complex (double line) connection between block is labelled with a C. The blocks designated 120, 148, 166, 192, 250 denote the change of representation of a complex signal from a single line labelled complex at an input thereof, which in reality is two lines, into two separate lines (real and imaginary) at an output thereof. The blocks designated 104, 146, 150, 224, 264 denote the change of representation of a complex signal from two separate lines (real and imaginary) at a respective input thereof, into a signal represented by a single line labelled complex at an output thereof, which in reality represents two lines.

Before considering the full architecture of the cancellor based on the comprehensive Rake architecture, it will be helpful to discuss the original Comprehensive Rake receiver disclosed in GB Patent Application No 9311373.6, the contents of which is incorporated herein by reference thereto. The parallel architecture will only be briefly described hereafter with reference to Figure 1.

Referring to Figure 1, a parallel comprehensive Rake receiver is shown for use with Binary Phase Shift Keying with Quadrature Phase Shift Keying randomisation. The receiver comprises a number of Rake fingers 2 - 10 each comprising a complex digital correlator 12 for handling a pilot signal and a complex digital correlator 14 for handling the data signal. The complex digital correlator 12 generates two output signals which are applied to an input of a Wiener like filter 16, 18 respectively. The complex digital correlator 14 has two output lines connected to an input of a delay device 20, 22 respectively. The output lines from the delay circuits 20, 22 are connected to an input of a linear multiplying circuit 24, 26 respectively. Each multiplying circuit has a further input connected to an output of the Wiener like filters 16, 18 respectively. The output from the Wiener like filters are also connected to the inputs of two further linear multiplying circuits 28, 30 each of which have both of their inputs connected to an output of the Wiener like filter. An output from each of the multiplying circuits 24, 26 is connected to an adder circuit 32, the output of which is connected to a first input of a switching device 34. The outputs from the multiplying circuits 28, 30 are connected to an input of a further adder circuit 36, the output of which is connected to an input of an alpha tracker circuit 38. An output from the alpha tracker circuit 38 is applied to a threshold device 40, the output of which is used to control the operation of the switch 34, the output of the switch 34 is connected to an input of a further adder circuit 42 which also receives the respective

outputs from the other Rake fingers 4 - 10. The output generated from the adder circuit 42 represents the received data signal.

A complex shift register 43 receives the input signal to the Rake receiver and each successive bit of the shift register is connected to one of the Rake fingers to an input of the complex digital correlators 12 and 14.

The operation of the circuit shown in Figure 1 will be described.

Each Rake finger 2 - 10 is subjected to a successive one chip delayed version of the input signal as that signal is passed through the complex shift register 43. The complex digital correlators 12 and 14 are used to de-spread the in-phase I and the quadrature phase Q components of that part of the signal arriving at the relevant time. In each case an I component is passed to a Wiener like filter 16 from the correlator 12, and to the delay circuit 20 from the correlator 14. Similarly the Q component is passed to the Wiener like filter 18 from the correlator 12 and to delay circuit 22 from the correlator 14. The Wiener like filters give good estimates of the I and Q values corresponding to the received signal element of the time one bit earlier than the input. The multiplying circuits 24, 26 are linear multipliers and each multiply an output of a respective Wiener like filter with an output from a respective delay device and the product from each multiplying device is summed by the adder circuit 32. The linear multipliers 28, 30 square the output from the respective Wiener filters 16, 18 and the product from each multiplying device is summed by the adder 36 and passed to the

input of the alpha tracker circuit 38. The alpha tracker circuit 38 is a digital equivalent of an RC low pass filter. The output from the alpha tracker circuit 38 is compared with a threshold by the threshold device 40 to determine when the signal component should be included in the overall combiner, and the switch 34 is caused to operate to pass the output from the adder circuit 32 to the adder circuit 42 which is used to combine the respective outputs from the other Rake fingers.

In the configuration shown in Figure 1, whenever the switch 34 is open, the complex digital correlator 12, the delay circuits 20, 22, the multipliers 24, 26 and the adder circuit 32 can be disabled. This will permit a smaller number of the circuit elements to be shared across all the Rake fingers because only about one third of all switches will be closed at any one time.

For cancellation of multiple interfering signals, a pre-combining Rake architecture is more appropriate. The comprehensive Rake architecture is easily modified to this form. The pre-combining Rake receiver can take one of two forms depending on where the QPSK randomising code is removed. The block diagram shown in Figure 2 considers the case where the QPSK randomising code is removed before combining over the multipath components.

It will be appreciated that the block diagram shown in Figure 2 is virtually identical to that shown in Figure 1. Therefore, like elements have been given the same designation. The difference between Figure 1 and Figure 2 is that the complex digital correlator 14, shown in Figure 1, is replaced by a complex

modulator 44, employing a phase randomising code. The output from the adder circuit 42 is applied to three real signal correlators A, B and C designated 46, 48 and 50 respectively, to generate three received data signals designated A, B and C.

The operation of the circuit is as follows. The signal, in complex form and sampled at one sample per chip, enters the complex shift register 43. Each point along the shift register feeds off to a Rake finger 2 - 10. Without loss of generality, the operation of the Rake finger is described only.

The signal is divided into two paths, one for pilot energy extraction via the correlator 12 and the other for signal weighting via the modulator 44. The complex signal samples are correlated against the complex spreading sequence corresponding to the pilot code in the correlator 12. The correlator 12 produces real and imaginary (I and Q) components of the estimates of the response of the combined channel plus transmit and receive filters at that time. The quality of the estimates is improved by the Wiener filters 16, 18 as described in co-pending GB Patent Application No 9304901.3 which are of the symmetrical type and therefore introduce a delay (D1).

In the signal path the phase randomising signal is removed by means of the complex modulator 44. Note that this circuit is not a correlator, i.e. there is no integration or averaging function. After removal the phase randomisation , a delay is inserted to compensate for the delay in the Wiener like filters by delay circuits 20, 22. The Wiener like filter outputs provide an estimate of the channel phase and amplitude in cartesian form. This is

used to compensate the phase and weight the amplitude of the signal for this particular Rake finger. Since the phase randomisation has been removed the real component of the channel phase compensated signal is only of interest. The corresponding real and imaginary components of the signal are multiplied against the real and imaginary components of the channel estimate respectively by the linear multiplier 24, 26 the output from which are added by the adder circuit 32. This produces an output at the chip rate. Note that this circuit differs fundamentally from that of Figure 1, in that in the latter, outputs are generated at the bit rate.

The decision as to whether to add the signal component into the sum is determined on the basis of the overall energy in the pilot for this sample timing. The modulus squared of the pilot is formed by adding together the output of the two squarer circuits, the linear multipliers 28, 30. The addition is performed by the adder circuit 36. The signal energy is then averaged using an alpha tracker circuit 38 and compared against a threshold by the threshold device 40. When the signal exceeds a threshold, the switch 34 is closed and the signal is forwarded to the overall adder circuit 42. The overall adder circuit 42 produces an output at the chip rate which requires only a simple real correlation to de-spread (and hence demodulate) any required signals from the common transmission source. In the example of Figure 2, three wanted signals A, B and C are demodulated, although any number of signals may be demodulated. These three signals are de-spread in the circuits real signal correlator A, 46, real signal correlator

B, 48 and real signal correlator C, 50.

A cancellor based on the pre de-randomising comprehensive Rake receiver will now be described with reference to Figure 3. The upper part of the diagram is identical to Figure 2 except for the addition of adder circuit 52 for the pilot energy squared which is switched to the adder circuit via a switch 54. This is required to scale the measured interfering signal energy level as described in GB Patent Application No 9313078.9. Just as in Figure 2, the output of the pre-combined Rake adder circuit 42 feeds the real signal correlators for demodulation of the wanted signals, so in Figure 3 the Rake combiner output is connected to a corresponding interferer demodulator and re-modulator 56, 58. In general there will be plurality of these correlators but two (A and B) are illustrated.

Each demodulator and re-modulator 56, 58 comprises the circuitry shown in Figure 4, which now will be described. A real interferer correlator demodulator 80 is connected to receive the output from the Rake receiver. An output from the correlator demodulator 80 is connected to the input of a half linear multiplying circuit 82 and to an input of a hard limiting device 84. An output from the hard limiting device 84 is connected to a further input of the half linear multiplying circuit 82 and to an input of a delay circuit 86. An output from the half linear multiplying circuit 82 is connected to an input of a linear multiplying circuit 88. A second input of the multiplying circuit 88 is connected to receive a reciprocal pilot energy signal. An output from the multiplying circuit 88 is connected to an input of

an averaging hold circuit 90, an output of which is connected to an input of a further linear multiplying circuit 94. An output from the delay circuit 86 is connected to an input of a real interferer A spreader 92, the output of which is connected to a further input of the multiplying circuit 94, the output of the multiplying circuit 94 generates real signals which are connected to an input of the adder circuit 62 of Figure 3.

The operation of Figure 4 is as follows. The real interferer correlator demodulator 80 demodulates the relevant interfering signal. Its output is then detected by the hard liming device 84 and fed, via a delay circuit 86 to the interferer A spreader 92 for the same spreading code which re-modulates the signal. The output from the correlator demodulator 80 is also fed to the input of the half linear multiplying circuit 86 in order to obtain the modulus of the received samples. These samples are then scaled by the reciprocal of the measured total pilot energy by the half linear multiplying circuit 88 and averaged with an averaging period D2 by the circuit 90. After the averaging, the measured level is used to scale the re-modulated signal by the multiplying circuit 94. The mathematics describing the use of the reciprocal measured total pilot energy is described in detail in GB Patent Application No 9313609.1. The reciprocal pilot energy signal is generated from the adder circuit 52 of Figure 3 and scaled by the scaling circuit 60 of Figure 3.

At this stage the QPSK phase randomisation has not been applied. Because this is common to all transmissions from a common base station, it can be applied after the various re-

modulated signals have been added together. Thus a real addition is performed across the two (or plurality) of re-modulated interfering signals by the adder circuit 62 of Figure 3. After this, the randomising code is added by the phase randomiser 64, and is shown in Figure 5.

Referring to Figure 5, the phase randomiser comprises a pair of half linear multiplying circuit 96, 98 each of which receive the real signal which is generated from the adder circuit 62 of Figure 3. The multiplying circuit 96 receives an I code from the I code generator 100, and the multiplying circuit 98 receives a Q code from the Q code generator 102. Each multiplying circuit 96, 98 generates an output signal which is connected to an input of block 104 which provides a complex output signal which is presented to an interference processor 70 of Figure 3.

The phase of the code is not shown but can be taken to be aligned appropriately with the re-modulating codes.

Having obtained the re-modulated complex baseband of the sum of several interferers, this must now be processed to obtain the equivalent signal which has passed through the following stages: transmit filter, radio channel, receive filter and Rake processor. This processing is performed in the interference processor 70 of Figure 3. This processing can take several forms. The first is shown in Figure 6.

Referring to Figure 6, the interference processor comprises two cascaded complex finite impulse response filters. The first filter comprises filters 122, 124, 126 and 128, the reverse order circuits 116, 118, block 120, the subtractor 130 and adder 132.

The second complex finite impulse filter comprises the filters 134, 136, 138 and 140, the adder 142, subtractor 144 and the block 146.

The block 120 has an input connected to the output of the phase randomiser 64 of Figure 3. The block 120 has two output lines, a first of which handles the real signals and is connected to the input of the filters 122, 124. The second output handles the quadrature phase signals and is connected to the inputs of the filters 126 and 128. An output of the filter 122 and the output of the filter 128 is connected to the inputs of the subtractor 130, and the output of the filter 124 and the filter 126 is connected to the inputs of the adder 132. The output of the subtractor 130 is connected to an input of the filter 134 and the filter 136, and the output of the adder 132 is connected to the input of the filter 138 and the filter 140. The output of the filter 134 and the filter 140 is connected to an input of the adder 142 and an output of the filter 136 and the filter 138 is connected to the inputs of the subtractor 144. The output of the adder 142 and the subtractor 144 are connected to an input of the block 146 respectively, the output of which is connected to an input of the phase de-randomiser 72 in Figure 3.

The interference processor also includes circuitry 106 which separates out the various components received from various parts of the circuit in Figure 3, which will be described in detail later. The I taps are connected to threshold circuit 108 and a gating circuit 112. The measured energy is connected to the threshold circuit 108 and the threshold circuit 110. The Q taps are

connected to the threshold circuit 110 and the gating circuit 114 and the gate signals are connected to the gating circuit 112 and the gating circuit 114.

The output from the threshold circuits 108, 110 are connected to inverters 116, 118 respectively, which inverts their output. The output from the inverter 116 is connected to a further input of the filter 122 and the filter 126. The output of the inverter 118 is connected to a further input of the filter 124 and to a further input of the filter 128. The output from the gating circuit 112 is connected to a further input of the filter 134 and to a further input of the filter 138. The output from the gating circuit 114 is connected to a further input of the filter 136 and to a further input of the filter 140.

Referring to Figure 6, block 106 simply routes the various elements of the bus from the Rake fingers into the separate categories. The I taps come from the Wiener like filter 16 in Figure 3 and the Q taps from the Wiener like filter 18 in Figure 3. The measured energy is the output of the alpha tracker circuits 38 in Figure 3. The gate signals are the outputs of the thresholding circuits 40 from the individual Rake fingers in Figure 3.

The processing consists of two cascaded complex finite impulse response filters as described above. The first filter corresponds to the channel cum receive and transmit filters response while the second corresponds to the Rake processor. The processing is based on the fact that the Wiener filters provide estimates of the sampled impulse response of the channel cum transmit and receive filters. However, the samples are in reverse

order so their order is inverted prior to use by the inverters which reverse the order 116, 118. The additions and subtractions on the output of the second complex filter are carried out by the adder 142 and the subtractor 144, reversed to reflect the fact that the Rake processor applies the (time reversed) complex conjugate of the channel cum transmit and receive filters.

Some of the Wiener filters will contain so little signal component that their inclusion in the combined output would introduce more noise than signal. This applies also to the cancellation process. Thus when the signal is passed over the estimated channel model the aim is to generate a synthetic received signal the mean square error of which, from the actual signal is as small as possible. Suitable thresholding for this criterion will be different from the criterion for the Rake combiner. Hence, two different thresholding/gating circuits 108, 110 are included. A useful value for the first threshold would be equivalent to double the noise energy at the output of Rake fingers with no correlated signal component at its input. Thus the apply threshold circuits, compare the individual measured energy with a threshold and, depending upon whether or not the threshold is exceeded, output the corresponding I and Q taps or set them both to zero.

The appropriate value for the second threshold is identical to that used in the Rake fingers (since the second complex filters is intended to emulate the Rake processor). Accordingly, the gating signal from the corresponding Rake finger is used for this purpose, and applied by the gating circuits 112, 114.

An alternative interference processor is shown in Figure 7.

Referring to Figure 7, the alternative interference processor comprises a block 148, which is connected to receive the output of the phase randomiser 64 in Figure 3, and has two output lines, one of which is connected to the input of the filter 156 and the filter 157 for handing the real signals, and the second output is connected to an input of the filter 158 and 160 for handling the quadrature phase signals. The outputs from the filters 156, 160 are connected to an input of a subtractor 162 respectively, and the output from the filter 157 and 158 are connected to an input of an adder 164 respectively, the outputs of the subtractor 162 and the adder 164 are connected to an input of the block 150 respectively. The output of the block 150 is connected to the phase de-randomiser 72 in Figure 3. A processor 152 is connected to a further input of the filters 156 and 158, and a processor 154 is connected to a further input of the filters 157 and 160. Both these processors receive input signals from various points in Figure 3 to be described below.

The interference processor of Figure 7 essentially performs the same functions as that shown in Figure 6, except that a complex convolution is performed across the coefficients of the first and second filters in order to generate the taps of a single, double length, complex filter. This is performed by the processors 152, 154. Under most circumstances this combined filter approach will be more complex than the separate filter approach because of the need to regularly update the coefficients of the common filter. However, it may have advantages in terms

of the precision of arithmetic required or may provide a better match to the available technology in terms of specific processing circuits for finite impulse response filtering.

Following the interference processing, cancellation is now necessary, ideally at the output of the pre-combining Rake circuit. However, the latter has already removed the QPSK randomising code, whereas the synthetic interfering signals still carry it. Thus it must first be removed. Since the synthetic interfering signal have been nominally co-phased by the Rake component of the interference processor, only a half complex de-randomisation process is required. The block diagram of the phase de-randomiser 72 of Figure 3 is shown in Figure 8.

The phase de-randomiser comprises a block 166 which receives at an input thereof the output from the interference processor 70 of Figure 3. The block 166 has two output lines, the first of which is connected to the first input of a half linear multiplying circuit 172, having a second input at which an output from an I code generator 168 is received. A second output line of the block 166 is connected to a first input of a half linear multiplying circuit 174, having a second input at which an output from a Q code generator 170 is received. The output lines of the multiplying circuits 172 and 174 are connected to an input of the subtractor 74 of Figure 3.

At this stage it might seem that the addition and removal of the phase randomisation in the interference path is pointless because the second operation cancels the first. In the absence of multipath this would be true but there will be cross multipath and

cross phase components generated through the addition and removal of the phase randomisation which would not be produced otherwise. Since these components will also be produced in the main signal path they must be generated here too for effective cancellation.

Having produced the suitably processed interfering signals they can be subtracted from the Rake combiner after an appropriate delay in order to effect cancellation by the subtractor 74 in Figure 3. After the cancellation operation, any number of wanted signals, two shown in Figure 3, can be demodulated using simple real correlators 76, 78 in Figure 3.

A pre-combining comprehensive Rake receiver which utilises post de-randomising will be described with reference to Figure 9. In this type of Rake receiver the QPSK phase randomisation is removed after the combining of the various multipath components.

Referring to Figure 9, a number of Rake fingers 180 - 186 is shown and the circuitry will now be described with reference to Rake finger 180 but it will be appreciated by those skilled in the art that the circuitry is identical in all Rake fingers.

Each Rake finger comprises a complex digital correlator 190 for handling a pilot signal, and a block 192 for receiving the complex signal from a complex shift register 188, external to the Rake finger. It will be appreciated that each Rake finger receives a subsequent chip from the complex shift register 188.

The complex digital correlator 190 has two output lines each of which is connected to an input of a Wiener like filter 194, 196

respectively. The output lines from the Wiener like filter 194 is connected to a first input of a multiplying circuit 202, to first and second inputs of a multiplying circuit 214 and to an input of a multiplying circuit 208. The output from the Wiener like filter 196 is connected to an input of a multiplying circuit 204, to two inputs of a further multiplying circuit 216, and to an input of a multiplying circuit 206. The block 192 has two output lines, each of which is connected to a delay device 198, 200. The output from the delay circuit 198 is connected to a further input of the multiplying circuit 202 and to a further input of the multiplying circuit 206. The output from the delay circuit 200 is connected to a further input of the multiplying circuit 204 and to a further input of the multiplying circuit 208. The outputs from the multiplying circuits 202 and 204 are connected to an adder 210, the output of which is connected to a switch 226. The outputs of the multiplying circuits 206, 208 are connected to a subtractor 212, the output of which is connected to a switch 228. The outputs from the multiplying circuits 214 and 216 are connected to an adder 218 the output of which is connected to an alpha tracker circuit 220. The output of the alpha tracker circuit 220 is connected to a threshold device 222 the output of which is used to control the operation of the switches 226 and 228. A block 224 has two input lines, each of which is connected to respective switch 226, 228. The output of the block 224, together with the outputs of the same blocks in the other Rake fingers, are connected to an input of the adder circuit 230. The output of the adder circuit 230 is connected to an input of a phase de-

randomising circuit 232, the output of which is connected to a plurality of real signal correlators 234, 236, 238, the outputs of which generate the received data signal A, B and C respectively.

The operation of this receiver is very similar to that of Figure 2. Indeed it will give identical performance. However, in this architecture, phase de-randomisation is performed in one place, at the output of the Rake combiner adder circuit 230. The phase de-randomising block is the same as that shown in Figure 8. The other difference is that the overall Rake combiner must now be complex. This is because there is information related to the signal(s) in both the in-phase and the quadrature components. Moreover, this means that the phase compensation applied from the pilot measurements in each Rake finger must also be fully complex, requiring four, rather than two multiplications. Thus, the complex phase de-randomiser in each Rake finger requiring four half multipliers, linear on one port only, plus a half complex multiplier have been replaced with one full complex multiplier. On first sight this may not appear advantageous. However, if conceptually, the complex shift register is split into three parallel complex shift registers with a common single input then the additional complex shift registers can be viewed as part of a pair of half complex finite impulse response filters. The architecture then becomes as shown in Figure 10, where the same components have been given the same reference numerals as shown in Figure 9.

It will be seen with reference to Figure 10 that each Rake finger is now very much less complex than that shown in Figure 9.

However, the reduced complexity in each Rake finger now involves the requirement of a further delay circuit 240 to delay the input signal.

Each of the four multipliers of the Rake fingers in Figure 10, are in the new architecture, grouped with their corresponding multipliers from the other Rake fingers to form a set of four real finite impulse response filters. The complex Rake filter 242 is implemented as shown in Figure 11.

Referring to Figure 11, it will be appreciated that the circuit is very similar to the right hand part of Figure 6 and functions in the same manner. The elements 244 - 268 operate in the same manner as the elements 106, 112, 114, 120, 134 - 146 of Figure 6 and therefore further description is not necessary. The obvious difference being that the block 250 has its outputs connected to the input of the filters 252, 254, and a second output thereof connected to the inputs of the filters 256, 258.

Although marginally more complex than the other architecture, this form has considerable advantages. The major benefit is in the fact that the heaviest processing burden is distilled into the four real finite impulse response filters, for which optimised high performance integrated circuits are available.

A cancellor based on the post de-randomising comprehensive Rake receiver will now be described with reference to Figure 12.

The cancellor based on a pre-combining comprehensive Rake including post de-randomising includes a pilot based

estimator 266 which receives a complex baseband input signal. This signal is also applied to a delay device 268, the output of which is connected to an input of a complex Rake filter 270, the various outputs from the pilot based estimator 266 is connected to inputs of the complex Rake filter 270 and to a further delay device 272. The pilot based estimator 266 also generates a real signal output which is connected to a scaling device 274. An output from the complex Rake filter 270 is connected to an input of a delay device 276 and to an input of a phase de-randomiser 278. The phase de-randomiser 278 generates a real output signal which is connected to an input of an interferer de-modulator and re-modulator 280 and to an input of an interferer de-modulator and re-modulator 282. The de-modulators and re-modulators 280, 282 also receive an output signal from the scaling device 274. The de-modulator and re-modulator 280, 282 each generate an output signal which is applied to an input of an adder device 284 respectively, the output of which is connected to a phase randomiser 286. An output from the phase randomiser 286 is connected to an input of an interference processor 288, which also receives the various outputs from the delay device 272, and produces a complex output signal which is applied to a subtractor circuit 290 which also receives the output signal from the delay device 276. The output from the subtractor device 290 is connected to an input of a further phase de-randomiser 292, the output of which is connected to an input of real signal correlators 294, 296 from which the output signals are generated.

In Figure 12, the pilot based estimator is essentially the same as the upper part of Figure 10. The only differences are the provision of an overall pilot energy measurement and the fact that the bus also includes the measured energy on the individual rake finger components. The actual details of the pilot based estimator are shown in Figure 13.

The pilot based estimator will now be described with reference to Figure 13. It comprises a plurality of Rake fingers 300 - 310 and it will be appreciated that each Rake finger includes identical circuitry to be described hereinafter with reference to Rake finger 300.

Each Rake finger includes a complex digital correlator for the pilot signal 312 which receives an input signal from a first bit of a complex shift register 314 external to the Rake fingers. It will be appreciated that each complex digital correlator in each Rake finger receives a delayed version of the input signal as its input is connected to a respective bit in the complex shift register 314. The complex digital correlator 312 generates two output signals, a real signal and a quadrature phase signal, each of which is applied to a respective Wiener like filter 316, 318. An output from the Wiener like filter 316 is applied to two inputs of a linear multiplying circuit 320, and the output from the Wiener like filter 318 is applied to both inputs of a linear multiplying circuit 322. The outputs from the Wiener like filters are also applied to a bus 324 for connection to the complex Rake filter 270 and the delay device 272 in Figure 12. The outputs from the linear multiplying devices 320, 322 are applied to an adder circuit 326, the output of

which is applied to an input of an alpha tracker circuit 328 and to a switch device 330. The output from the adder circuit 326 is also applied to the bus 324. An output from the alpha tracker circuit 328 is applied to an input of a threshold circuit 331, the output of which is used to control a switch 330, and is also passed to a bus 324. The other side of the switch 330 is connected to an input of an adder circuit 332, external to the Rake fingers. It will be appreciated that the adder circuit 332 receives an input from the respective other Rake finger circuits. The output of the adder circuit 332 generates a real signal which is applied to the scaling circuit 274 in Figure 12.

The operation of the cancellor is as follows. The pilot based estimator derives the Rake finger tap weights for the complex Rake filter. The output of this filter is suitably processed for multipath but still includes the phase randomisation component. This is removed by the phase de-randomiser 278 to allow de-modulation of the two, e.g. interferers A and B. The interferers de-modulator and re-modulator 280, 282 are as shown in Figure 4. The phase randomiser 286 and interference processor 288 operate as described above to produce phase randomised interfering signals suitable for cancellation. Since the output of the complex Rake filter has not been de-randomised, cancellation, following an appropriate delay, can be applied at this stage. Phase de-randomisation is now applied and the signals can be de-modulated as required.

Referring back to Figure 11, it may have been noted that the complex Rake filter shown in Figure 11 is identical to the second

half of the first interference process shown in Figure 6. This is expected, since the purpose of the second half of Figure 6 is to repeat the operations of the Rake filter. This fact points to an alternative architecture in which cancellation is performed prior to a second Rake processing operation. This is shown in Figure 14.

Referring to Figure 14, it will be appreciated that the circuit is quite similar to Figure 12 and like components have been given the same designation. The difference between the two circuits is the delay device 276 has its input connected to the output of the delay device 268 instead of the output of the complex Rake filter 270. A channel model circuit 334 is used instead of the interference processor 288 and a second complex Rake filter 336 is connected in between the output of the subtractor circuit 290 and the input of the phase de-randomiser 292. The complex Rake filter 336 also receives the outputs from the delay device 272. The channel model circuit 334 is also connected to the output of the delay device 272 and is identical to the first half of the interference processor as illustrated in Figure 6 and for clarity this is shown in Figure 15. The same reference numerals have been used throughout Figure 15 and it will be appreciated that the circuit functions in exactly the same manner as that described with reference to Figure 6. The output lines from the subtractor 130 and the adder 132 are connected to the inputs of the block 146.

The operation of this cancellor is basically the same as that of Figure 12. The only difference is the point at which the cancellation is applied. Indeed the performance and complexity of

the two will be essentially the same. The motivation for introducing this architecture at this stage is that it points the way to an architecture suitable for cancellation of signals from a different base station.

The architecture for an other base station cancellor is shown in Figure 16. A base station cancellor based on a pre-combining comprehensive Rake receiver for post re-randomising or pre-cancelling is shown in Figure 16. A complex baseband input signal is applied to an input of a pilot based estimator for a base station 1, 338 and to an input of a pilot based estimator for a base station 2, 340. The signal is also applied to a delay device 342. An output from the delay device 342 is applied to an input of a complex Rake filter from the base station 1, 334, which also receives output signals from the pilot based estimator 338. An output from the complex Rake filter 344 is connected to an input of a phase de-randomiser 346, the output of which is connected to an interferer de-modulator and re-modulator 348 and to input of an interferer de-modulator and re-modulator 350. The de-modulators and re-modulators 348, 350 also receive an output signal from a scaling device 352 which receives at an input thereof, a pilot energy signal from the pilot based estimator 338. An output from the de-modulators and re-modulators 348, 350 is applied to an input of an adder circuit 354, an output from which is connected to an input of a phase randomiser 356. An output from the phase randomiser 356 is connected to a channel model circuit 358 from base station 1. The channel model circuit 358 also receives signals from the pilot based estimator for base

station 1, 338 via a delay device 360. An output from the channel model circuit 358 is connected to an input of a subtractor device 362. The complex baseband input signal is also connected to an input of a delay device 364, the output of which is connected to a second input of a subtractor circuit 362. An output from the subtractor circuit 362 is connected to an input of a complex Rake filter from base station 2, 366 which also receives the output signals from the pilot based estimator for base station 2, 340 via a delay device 368. An output from the complex Rake filter 366 is connected to an input of a further phase de-randomiser 368, the output of which is connected to an input of a real signal correlator 370 and a real signal correlator 372, the outputs from which generate the output signals.

In Figure 16 it is assumed that there are two base stations 1 and 2. The interference, A.1 and B.2 comes from base station 1. The wanted signals, Rx1 and Rx2 both come from base station 2. In Figure 16, the two interfering signals are de-modulated, re-modulated by the circuits 348, 350 and processed by the channel model circuit 358 to obtain a delayed version of the signals at complex baseband. The lower half of Figure 16 shows a basic receiver for the wanted signals which includes a subtractor 362 for the interfering signals. An additional delay device 368 is included to allow for the processing time required to re-create the interfering signals.

Examination of Figure 16 indicates a possible improvement. If the cancellation is applied before the pilot based estimator for

the wanted base station then the signal to noise ratio of the pilot will be enhanced.

This is illustrated in Figure 17, which shows an other base station cancellor based on a pre-combining comprehensive Rake receiver. This architecture provides a modest improvement in performance at the expense of an additional delay device 374. In Figure 17 like circuit elements have been given the same reference numeral. However, as will shall see when considering a cancellor for signals from both the same and another base station, this benefit is obtained also at the expense of de-graded flexibility.

It will be observed that the pilot based estimator 340 does not receive the complex baseband input signal direct, but receives this signal via the delay device 364 and the subtractor 362. The output of the estimator 340 is passed directly to the complex Rake filter 366, which also receives a delayed version of the input signal to the estimator 340 via delay device 374. The operation of Figure 17 is similar to that described with reference to Figure 16.

Referring now to Figure 18, a cancellor is shown which provides cancellation from both base stations based on a pre-combining comprehensive Rake, utilising post de-randomising and pre-cancelling. It will be appreciated that this Figure is basically a combination of both Figures 14 and 16 and therefore like designations have been given to like circuit components. The block diagram shown in Figure 18 requires one further adder circuit 376 which combines the output signals from the two channel model circuits 358 and 334.

With reference to Figure 18, it is assumed that there are two base stations, 1 and 2. The interference, A.1 and A.2 comes from base station 1. The interference, A.2 and B.2 comes from base station 2. The wanted signals, Rx1 and Rx2 both come from base station 2. Further description of Figure 18 is unnecessary in view of the description earlier in relation to Figure 14 and Figure 16. The top half of the block diagram re-creates the interference from base station 1. The middle part re-creates the interference from base station 2. In the lower portion the re-created interference sources are added together prior to subtraction from the delayed received signal and final de-modulation.

It should be clear that the architecture of Figure 17 does not fit well with this approach since only one of the pilots can be cancelled and several compensating delays are required.

It will also be apparent that a minor extension to the architecture of Figure 18 would allow simultaneous reception, as well as cancellation from both base stations. Specifically, the addition of another complex Rake filter, from base station 1 on the output of the subtractor, followed by an appropriate phase de-randomiser, then various real signal correlators would allow reception of signals from base station 1 as well as base station 2. The complex Rake filter, from base station 1 would be fed from the delayed bus from the pilot base estimator of base station 1.

It will also be apparent to those skilled in the art that if no QPSK phase randomisation is applied, then setting the Q code generator outputs to zero will result in a half complex implementation suitable for cancellation and reception for this

kind of modulation, and subsequent redundant circuitry will be removed.

Alternatively, the Q code generator could be set to the same or inverse output as the I code generator to produce a half complex implementation.

CLAIMS

1. Apparatus for use in equipment providing a digital radio link, using direct sequence spread spectrum and including a pilot signal reference, between fixed and mobile radio units, said apparatus comprising a Rake receiver including a plurality of Rake fingers, each including means for measuring the amplitude of the pilot signal reference and means for weighting the amplitude in accordance with the measured pilot amplitude which cover a contiguous span of spreading code phases of the same order as the maximum delay spread of the signal to be received, first adder means connected to an output of each Rake finger and arranged to generate a combined output signal, correlation means connected to receive said combined output signal and arranged to demodulate said signal to reconstruct signals to be received, second adder means for generating a signal pertaining to total pilot signal energy, scaling means for scaling said total pilot energy signal, and, means for cancelling interference from at least one interfering source of known spreading code, wherein said cancellation means is arranged to receive output signals from said first adder means and from said scaling means.

2. Apparatus as claimed in claim 1, wherein said cancellation means includes an interferer demodulator and re-modulator for each expected interferer, and each interferer demodulator and re-modulator comprises a interferer correlator for demodulating an interfering signal, multiplying means connected to an output of

said interferer correlator arranged to generate a modulus of received samples, scaling means for scaling said samples by a reciprocal of measured total pilot energy derived from second adder means, averaging means for averaging said samples, and re-modulating means arranged to re-modulate the signal applied to said interferer correlator.

3. Apparatus as claimed in claim 2, wherein the output from each interferer demodulator and re-modulator is applied to summing means, the output of which is applied to phase randomising means comprising first multiplying means for combining said signal with an in-phase code, and second multiplying means for combining said signal with a quadrature phase code.

4. Apparatus as claimed in claim 2 or 3, wherein said cancellation means includes an interference processor comprising two cascaded complex finite impulse response filters.

5. Apparatus as claimed in claim 4, wherein said first finite impulse response filter comprises first, second, third and fourth filters, real signal components being connected to a first input of said first and second filters, imaginary components being connected to said third and fourth filters, subtractor means for subtracting an output from said first filter from an output from said fourth filter, adder means for combining an output from second filter with an output from said third filter, first threshold

means for receiving control signals, second threshold means for receiving different control signals and arranged to generate output signals dependent thereon, inverter means for inverting the output signals from said first and second threshold means, wherein said output signals from said first threshold means are applied to a second input of said first and third filters, and output signals from second threshold means are applied to a second input of said second and fourth filters.

6. Apparatus as claimed in claim 5, wherein said second finite impulse response filter comprises first, second, third and fourth filters, wherein said first and second filters receive at a first input thereof, the output signal from the said subtractor means, said third and fourth filter receive at a first input thereof, the output signal from said adder means, said first and third filters being arranged to receive at a second input thereof, control signals, and said second and fourth filters being arranged to receive at a second input thereof, different control signals, wherein the output signals from said first and fourth filters are applied to further adder means, for generating real signal components, and an output from second and third filters being connected to further subtractor means for generating imaginary signal components.

7. Apparatus as claimed in claim 4, wherein said interference processor comprises first, second, third and fourth filters, said first and second filters being arranged to receive real signal components at a first input thereof, and said third and fourth

filters being arranged to receive imaginary signal components at a first input thereof, first processing means for providing control signals to a second input of said first and third filters in respect of real filter co-efficients, second processing means for providing control signals to a second input of said second and fourth filters in respect of imaginary filter co-efficients, subtractor means arranged to receive an output from said first and fourth filters, for generating real signal components, and adder means arranged to receive an output signal from said second and third filters, for generating imaginary signal components.

8. Apparatus as claimed in any of the preceding claims 2 to 7, wherein said phase de-randomiser comprises a first multiplying means arranged to receive real signal components and to combine therewith a first code generated from a first code generator, second multiplying means for receiving imaginary signal components and for combining therewith a second code generated by a second code generator.

9. Apparatus as claimed in claim 1, wherein each Rake finger comprises a pilot based estimator arranged to generate first and second output signals, the first of which is applied to a complex Rake filter, the second of which is indicative of measured pilot energy; said complex Rake filter having an output connected to first phase de-randomising means, an output of which is connected to a first and a second interferer demodulator and re-modulator which are connected to and controlled by an output

signal generated by scaling means which receives said measured pilot energy signal, said first and second interferer demodulator and re-modulator generate an output signal which is applied to phase randomising means which generates an output signal for application to processor means, said processor means being arranged to generate an output signal which is applied to subtractor means, which at a further input thereof receives an output signal from said complex Rake filter, second phase de-randomising means for receiving an output signal from said subtractor means and for generating an output signal which is applied to a plurality of signal correlator means arranged to reconstruct the received data signals.

10. Apparatus as claimed in claim 9, wherein said Rake filter comprises first, second, third and fourth filters, said first and second filter being arranged to receive real signal components at a first input thereof, and said third and fourth filters being arranged to receive imaginary signal components at a first input thereof, adder means arranged to sum an output from the said first filter with an output from the said fourth filter for generating real signal components, and subtractor means arranged to subtract an output of said second filter from an output of said third filter, for generating imaginary signal components, said first and third filters being arranged to receive control signals at a second input thereof, and said second and fourth filters being arranged to receive control signals at a second input thereof.

11. Apparatus as claimed in claim 9 or claim 10, wherein said pilot based estimator comprises correlation means for handling a pilot signal and generates real signal components for application to a first Wiener filter and imaginary signal components for application to a second Wiener filter, said first and second Wiener filters generate output signals which are applied to respective multiplying means for squaring said output signal, summing means for summing said squared signals and generating a signal to be applied to an input of tracking means, an output signal from said tracking means being applied to thresholding means for providing an output signal for controlling switching means for connecting said output signal from said summing means to a further summing means having a plurality of inputs each of which is connected to said output of each summing means in each Rake finger and is arranged to sum the output signals from each of the Rake fingers and generate an output signal for application to said scaling means, said output signals from said Wiener filters, said first summing means and said thresholding means being passed to bus means for application to said Rake filter.

12. Apparatus as claimed in claim 1, wherein each Rake finger comprises a pilot base estimator having an output connected to an input of a first Rake filter external to each Rake finger, an output of which is connected to first phase de-randomising means for generating input signals to first and second interferer de-modulator and re-modulators, said pilot base estimator generating

a further output signal for application to scaling means, said scaling means generating an output signal for controlling said interferer de-modulator and re-modulators, summing means for combining an output from each interferer de-modulator and re-modulator and an output thereof is applied to phase randomising means, the output of which is connected to an input of channel model means arranged to receive control signals from said pilot based estimator, subtractor means for combining an output from said channel model means with said baseband input signal and applying an output thereof to an input of a second Rake filter arranged to receive control signals from said pilot based estimator, said second Rake filter being connected to an input of second phase de-randomising means, an output of which is connected to a plurality of signal correlation means for reconstructing the received data signals.

13. Apparatus as claimed in claim 12, wherein said channel model means comprises first and second filters, each receiving at a first input thereof real signal components and third and fourth filters each receiving at a first input thereof imaginary signal components, an output from said first and said fourth filter being applied to subtractor means for generating real signal components, an output from said second and third filter being applied to adder means for generating imaginary signal components, said first and third filters being arranged to receive control signals in reverse order at a second input thereof, and said

second and fourth filters being arranged to receive different control signals in reverse order at a second input thereof.

14. Apparatus as claimed in claim 12 or claim 13, wherein said pilot based estimator is arranged to handle signals from a first base station and said first complex Rake filter is arranged to handle signals from said first base station, wherein a second pilot based estimator is provided for handling signals from a second base station, said second Rake filter is arranged to handle signals from said second base station, said channel model means is arranged to handle signals from said first base station, said second Rake filter being arranged to receive control signals from said channel model means and data signals from said second pilot based estimator.

15. Apparatus as claimed in claim 14, wherein said second Rake filter receives at an input thereof, an output signal from subtractor means which receives at a first input thereof said base band input signal, and at a second input thereof, an output signal from said channel model means.

16. Apparatus as claimed in claim 12 and claim 14, wherein a further channel model means is provided, and the output signal from each channel model means is applied to a respective input of adder means an output of which is applied to subtractor means, said subtractor means is arranged to receive said baseband input signal at a further input thereof, and providing an output signal

for controlling said second Rake filter which is arranged to handle signals from said second base station.

17. Apparatus as claimed in any preceding claim, wherein the interference is generated from a plurality of base stations.

18. Apparatus as claimed in claim 4, wherein the finite impulse response filters are half complex filters.

19. Apparatus substantially as hereinbefore described with reference to Figures 3 to 8, and 11 to 18 of the accompanying drawings.

Examiner's report to the Comptroller under Section 17 (The Search report)	GB 9317205.4
Relevant Technical Fields (i) UK Cl (Ed.M) H4P (PAL, PAN, PAQ, PRE, PRR, PDCSL); H4L (LBSF) (ii) Int Cl (Ed.5) H04L 27/22, 27/30, 27/38; H04B 7/216; H04S 13/00	Search Examiner K WILLIAMS
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ON-LINE DATABASE: WPI	Date of completion of Search 8 NOVEMBER 1993 Documents considered relevant following a search in respect of Claims :- 1-19

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

Databases:The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).